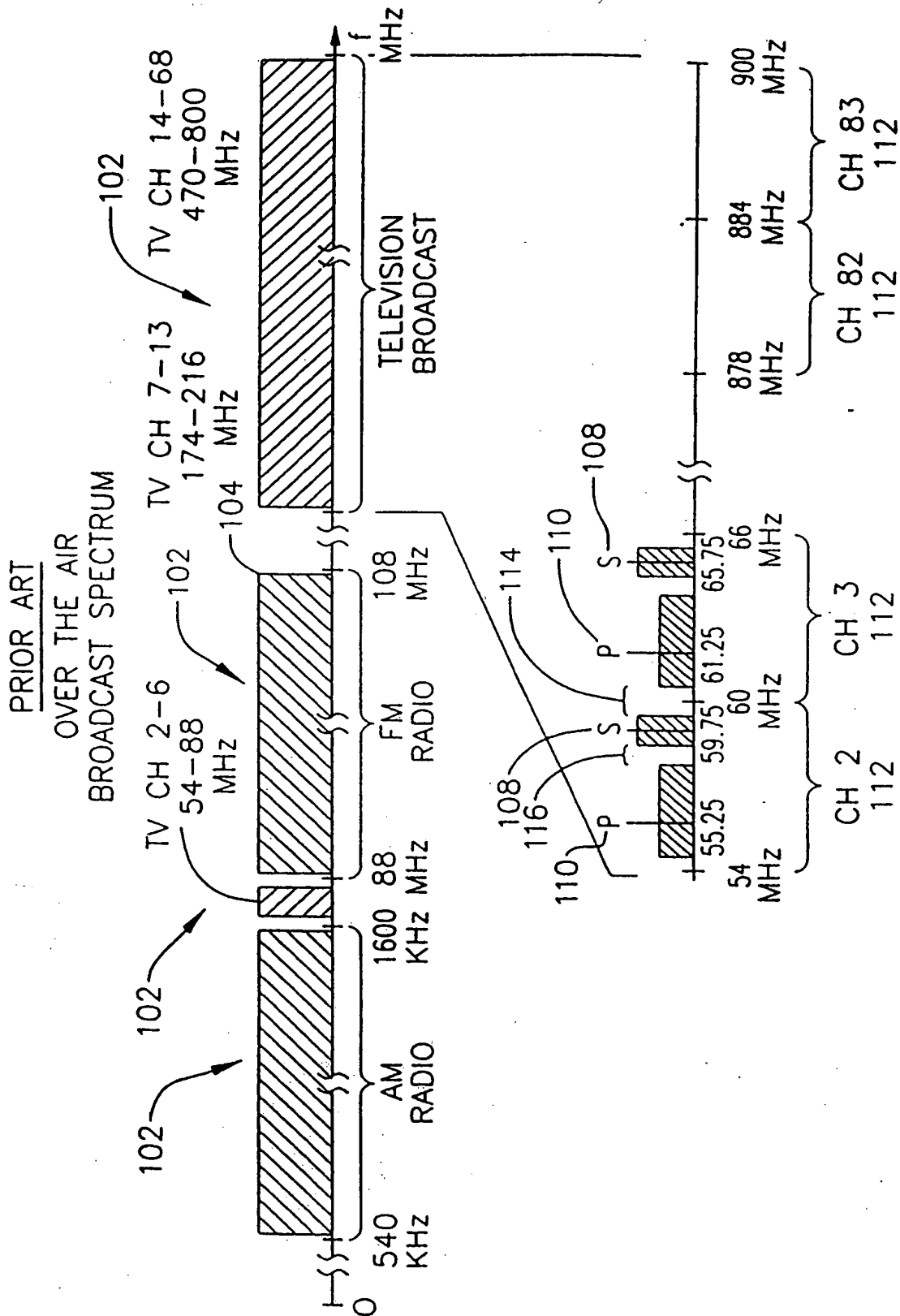
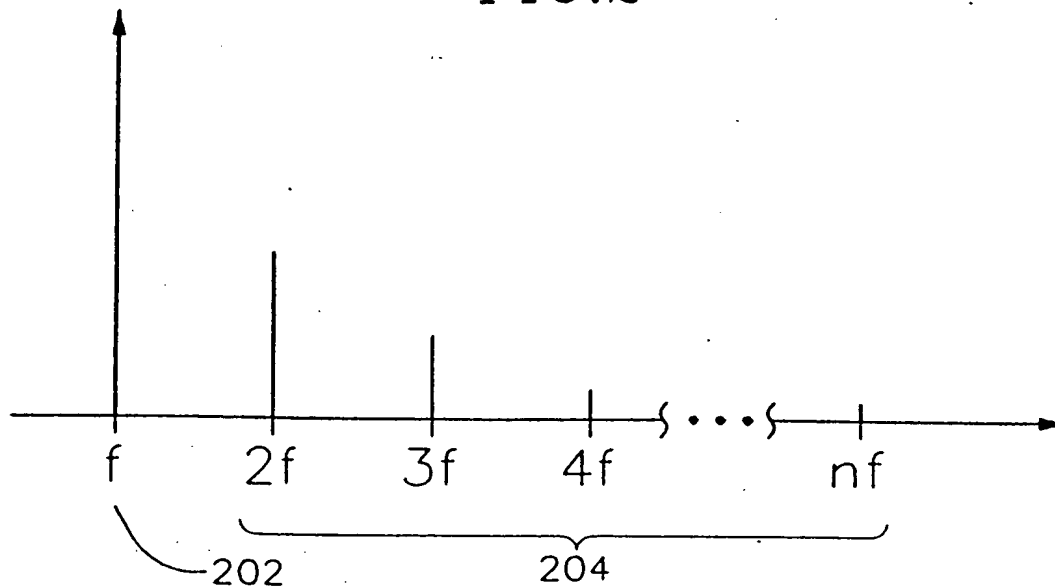


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 Dkt. No. 1875.138000G; Group Art Unit: To Be Assigned
 Inventors: Arya R. Behzad; Tel.: (202) 371-2600
 Title: Large Gain Range, High Linearity, Low Noise MOS
 VGA

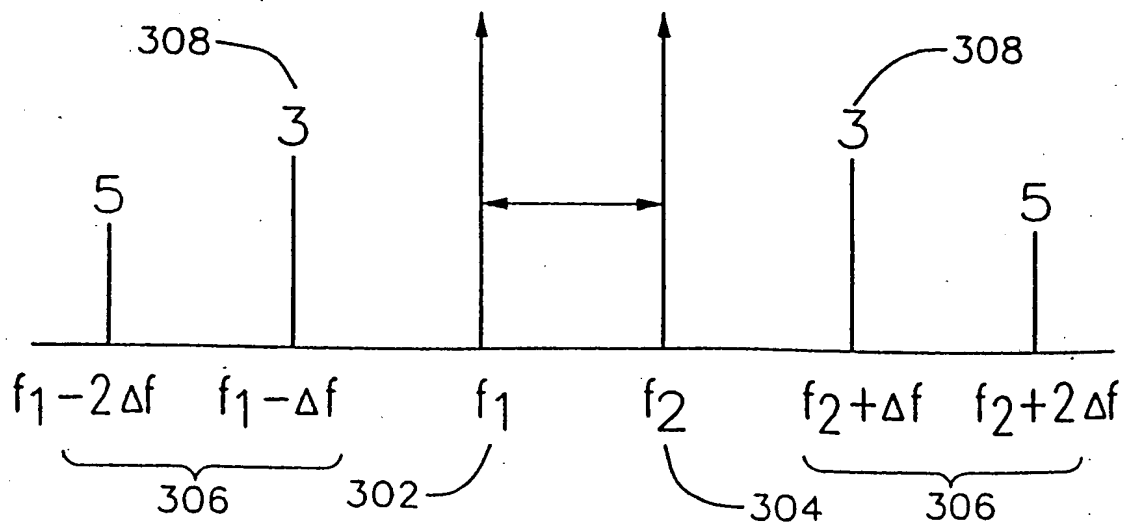
FIG. 1



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VGA

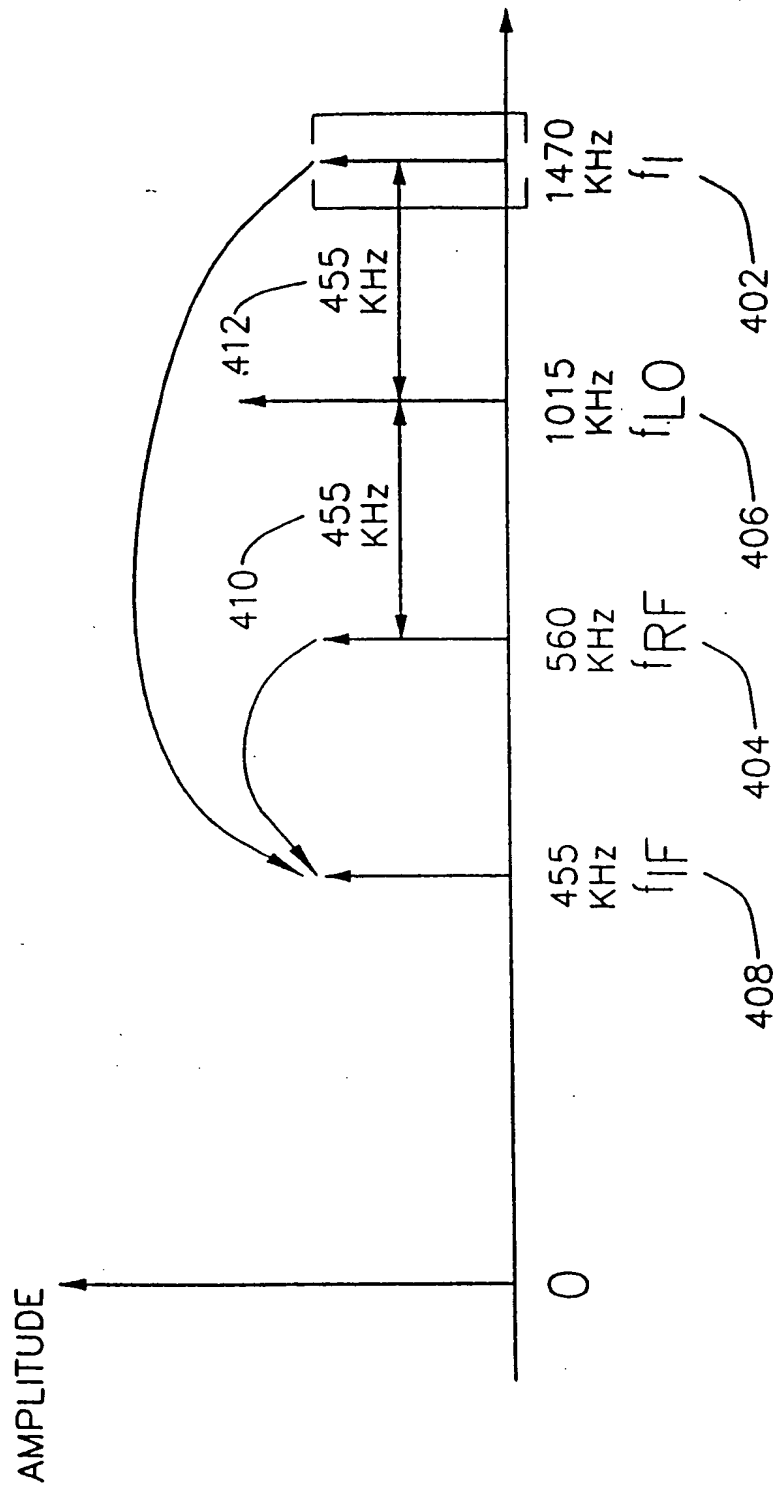
FIG. 2**FIG. 3**

PRIOR ART



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 VGA

FIG. 4
PRIOR ART



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 VGA

FIG. 5
 DUAL CONVERSION RECEIVER

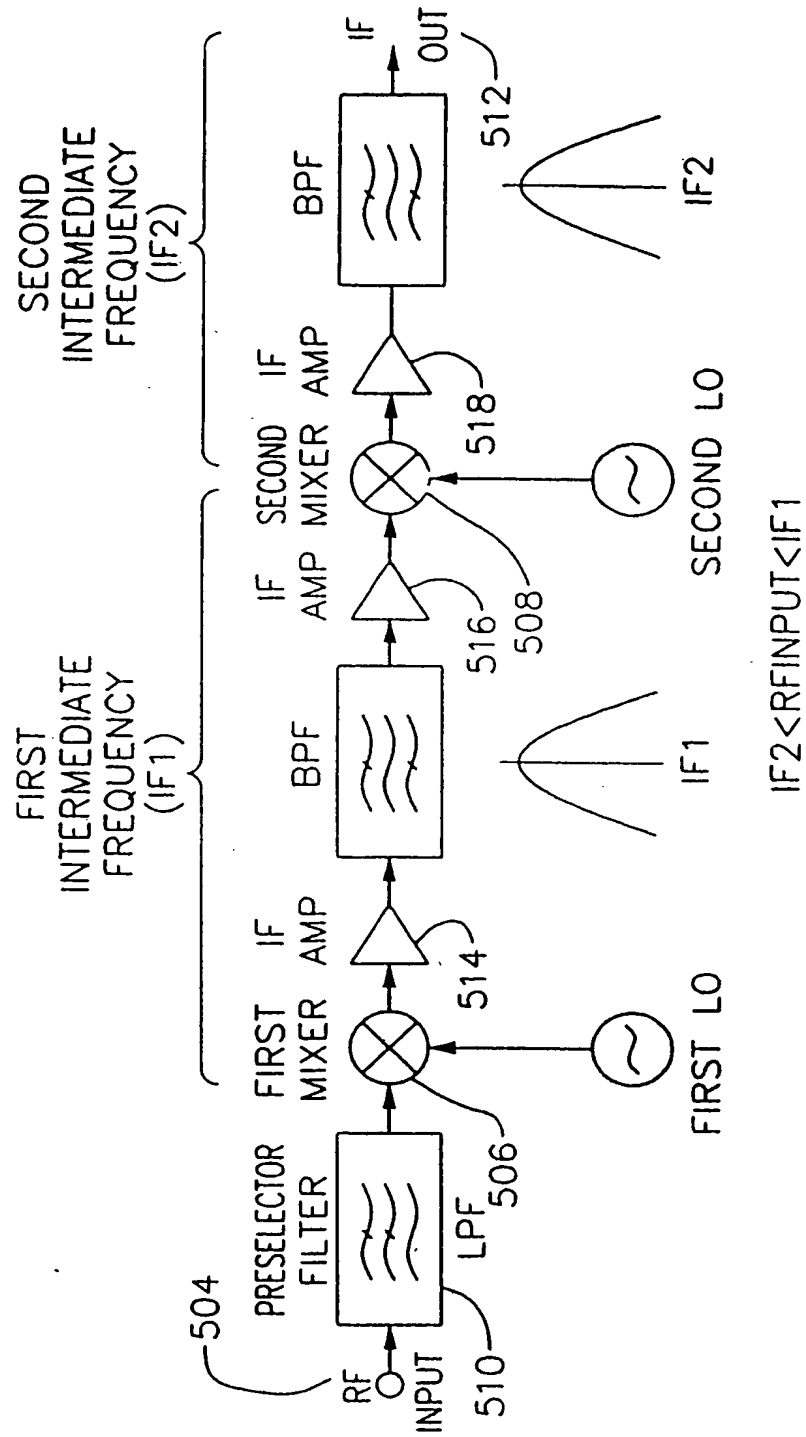


FIG. 6

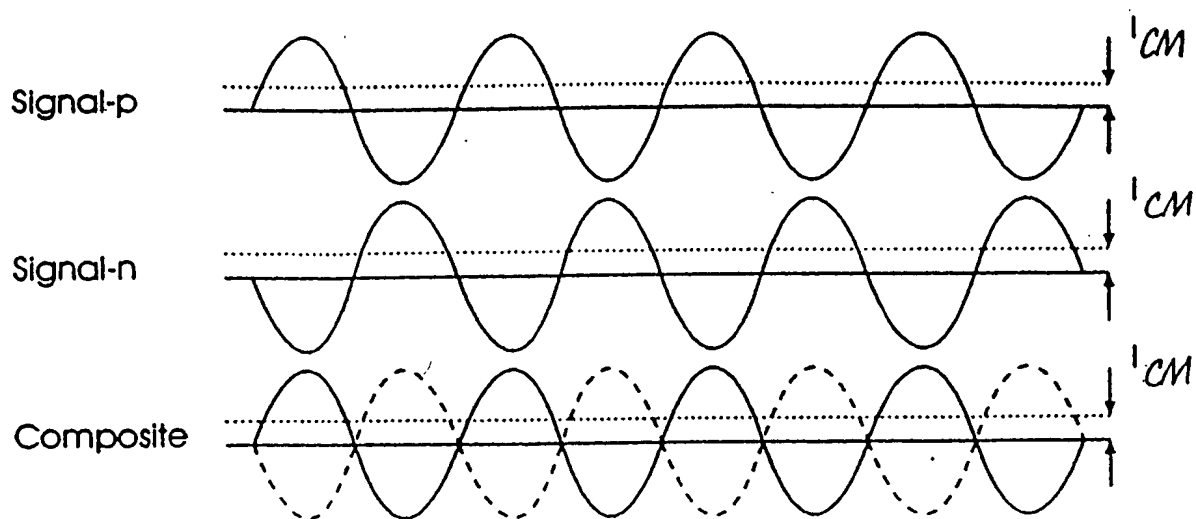
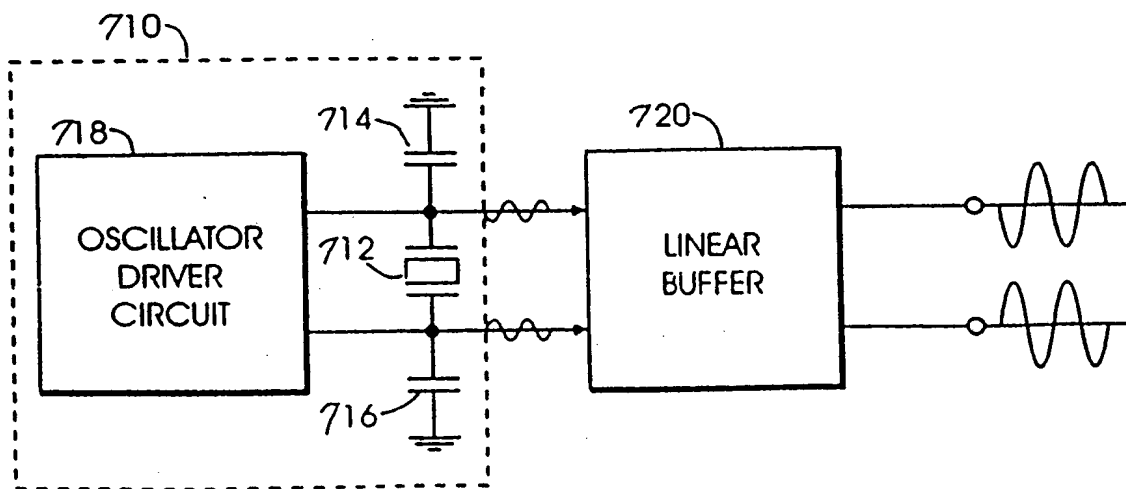


FIG. 7



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 Inventors: Arya R. Behzad; Tel.: (202) 371-2600
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 VGA

FIG. 8

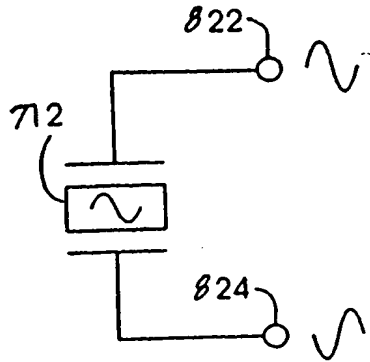


FIG. 9

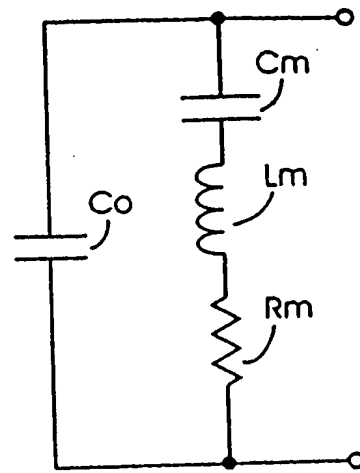


FIG. 10

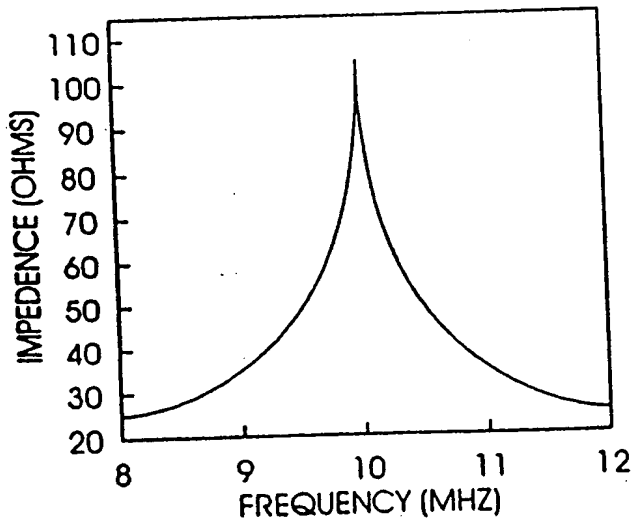
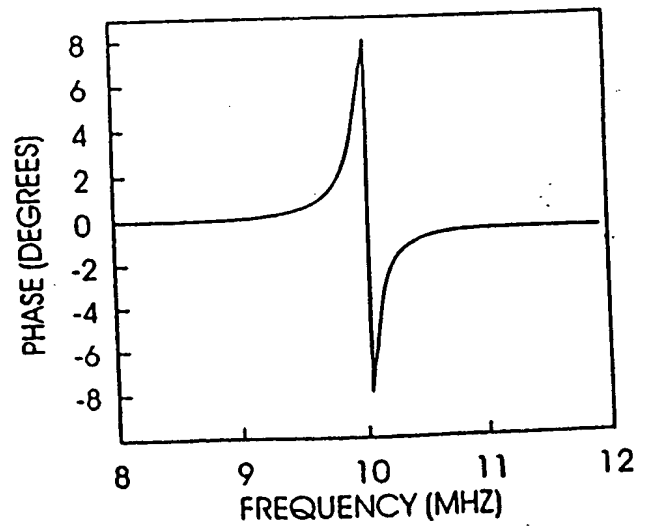


FIG. 11



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 Dkt. No. 1875.138000G; Group Art Unit: To Be Assigned
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FIG. 12

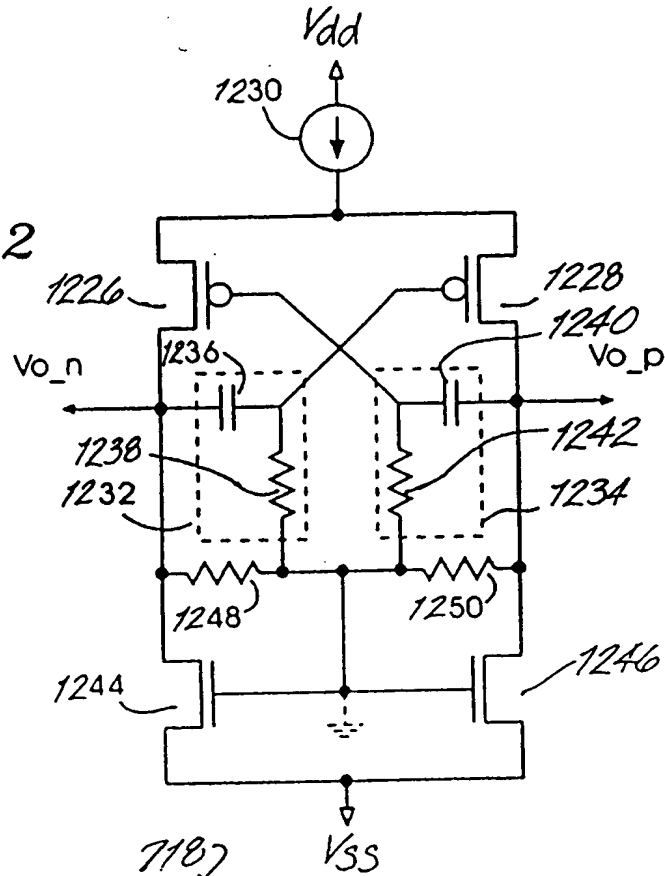


FIG. 13

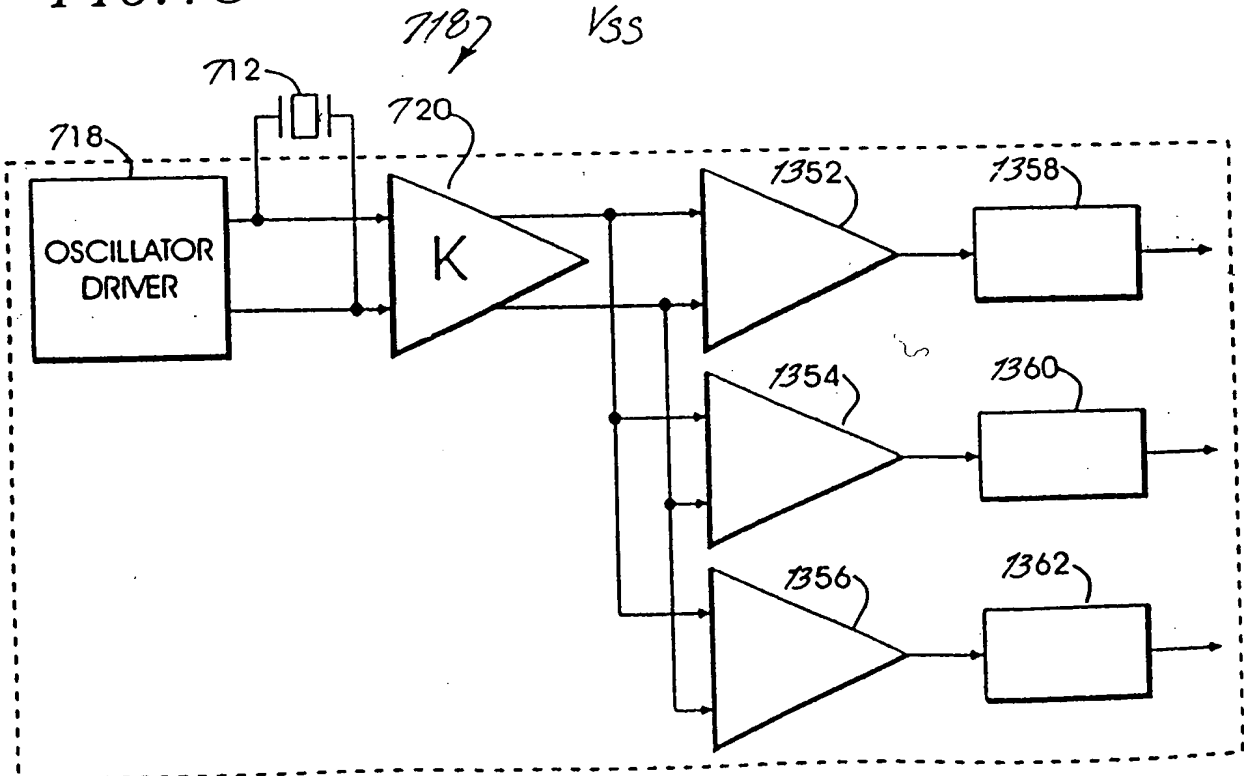
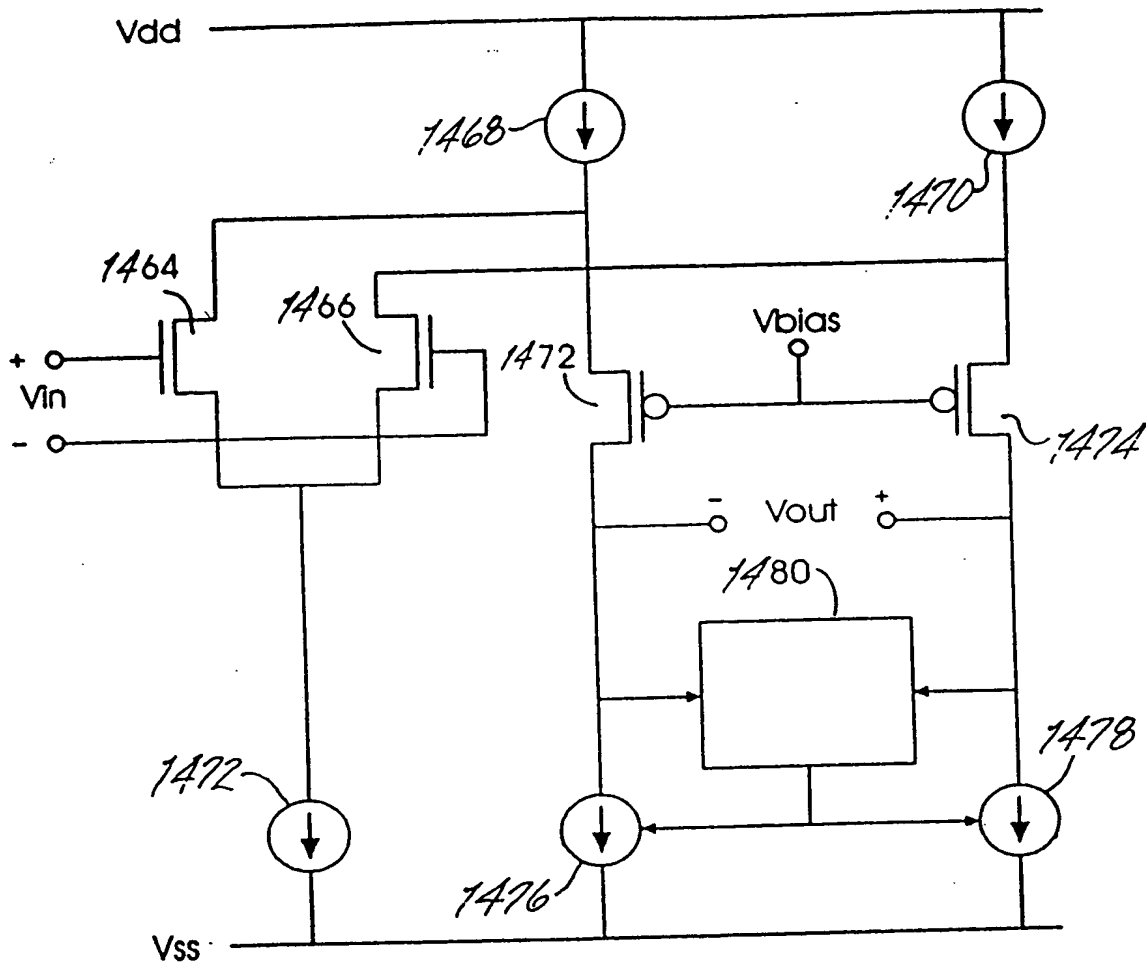


FIG. 14



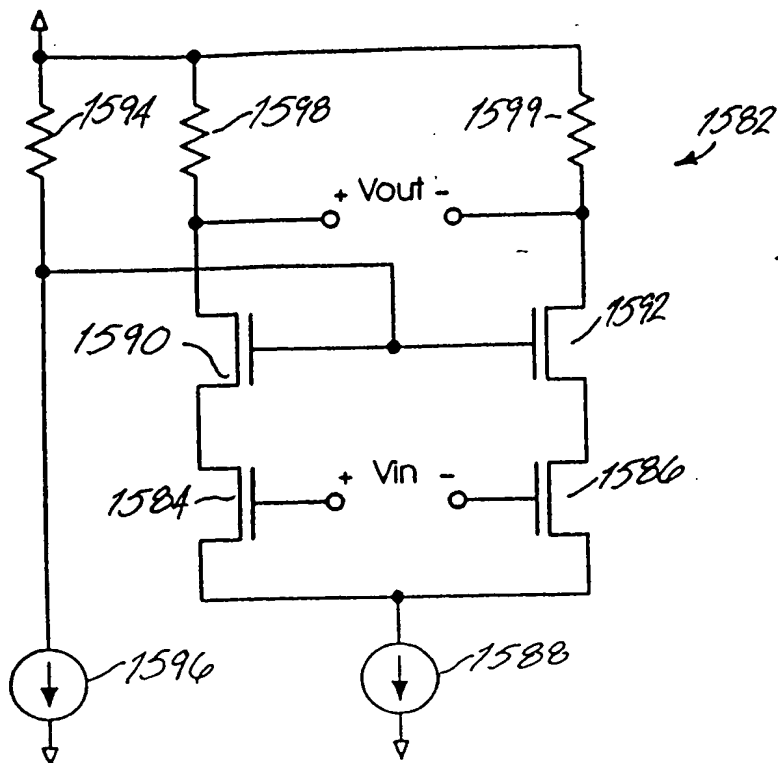
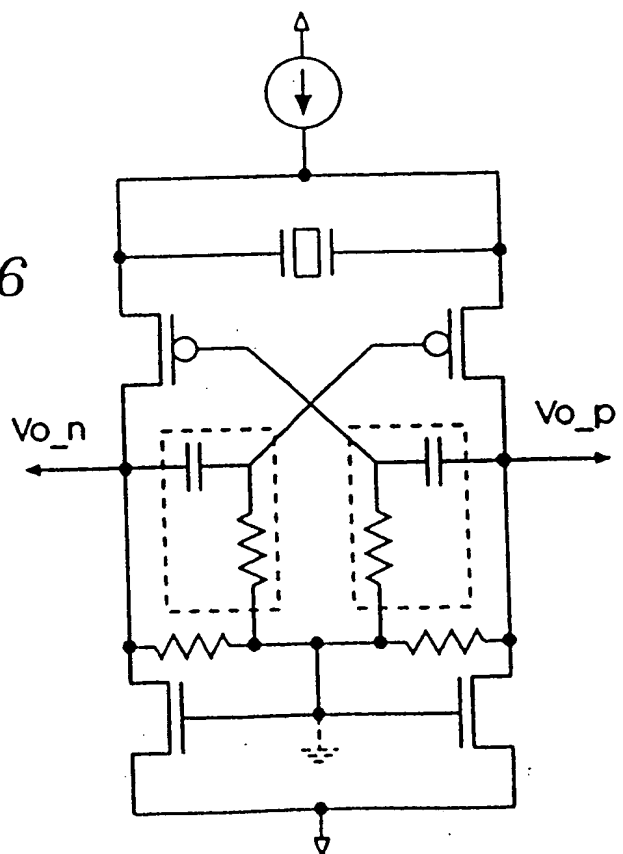


FIG. 15

FIG. 16



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 Dkt. No. 1875.138000G; Group Art Unit: *To Be Assigned*
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FIG. 17

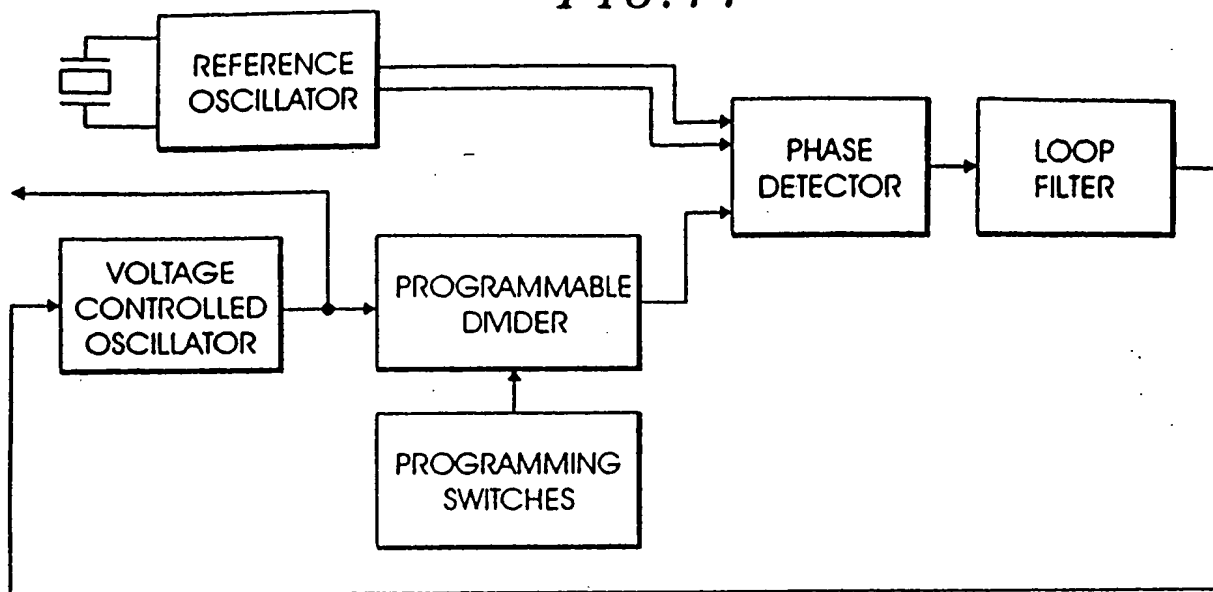
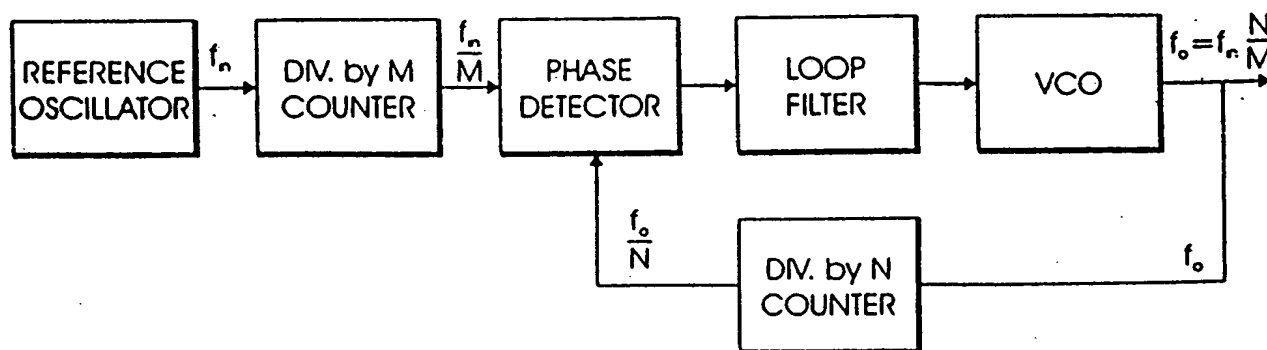


FIG. 18



UP CONVERSION DUAL DOWN CONVERSION

1906 50 860 RF 1912 1916 1908 1910 1930 1936 1948

FIRST MIXER SECOND MIXER THIRD MIXER

FILTER BANK #1 FILTER BANK #2 FILTER BANK #3

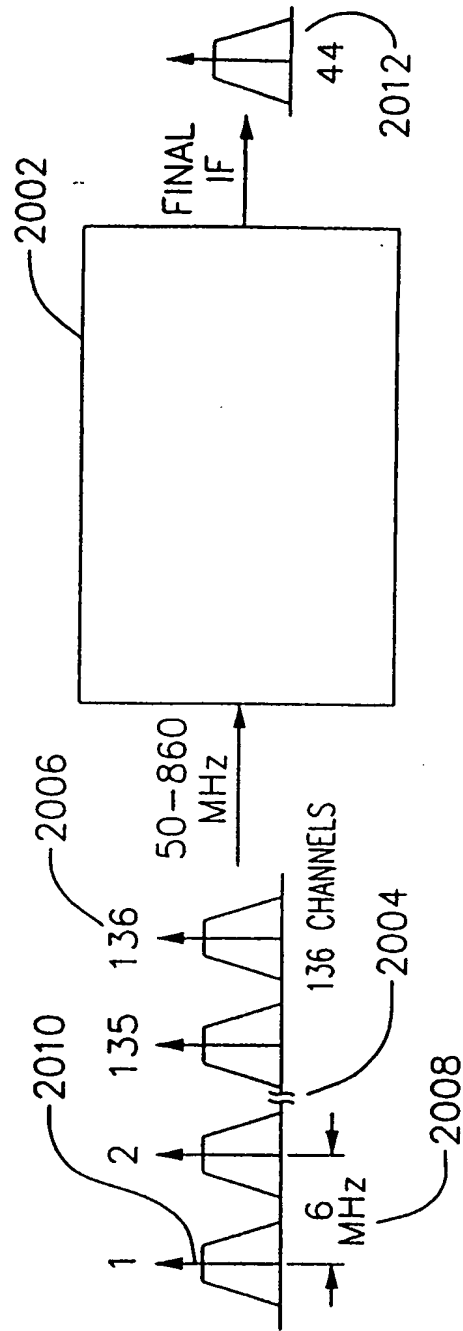
1200 MHz 275 MHz 36 OR 44 MHz

1250-2060 MHz 925 MHz 231 MHz

FIRST LO SECOND LO THIRD LO

1902 1904 1910 1912 1914 1916 1918 1920 1922 1924 1926 1928 1930 1932 1934 1936 1938 1940 1942 1944 1946 1948 1950 1952 1954 1956 1958 1960 1962 1964 1966 1968 1970 1972 1974 1976 1978 1980 1982 1984 1986 1988 1990 1992 1994 1996 1998 2000 2002 2004 2006 2008 2010 2012 2014 2016 2018 2020 2022 2024 2026 2028 2030 2032 2034 2036 2038 2040 2042 2044 2046 2048 2050 2052 2054 2056 2058 2060 2062 2064 2066 2068 2070 2072 2074 2076 2078 2080 2082 2084 2086 2088 2090 2092 2094 2096 2098 2100 2102 2104 2106 2108 2110 2112 2114 2116 2118 2120 2122 2124 2126 2128 2130 2132 2134 2136 2138 2140 2142 2144 2146 2148 2150 2152 2154 2156 2158 2160 2162 2164 2166 2168 2170 2172 2174 2176 2178 2180 2182 2184 2186 2188 2190 2192 2194 2196 2198 2200 2202 2204 2206 2208 2210 2212 2214 2216 2218 2220 2222 2224 2226 2228 2230 2232 2234 2236 2238 2240 2242 2244 2246 2248 2250 2252 2254 2256 2258 2260 2262 2264 2266 2268 2270 2272 2274 2276 2278 2280 2282 2284 2286 2288 2290 2292 2294 2296 2298 2300 2302 2304 2306 2308 2310 2312 2314 2316 2318 2320 2322 2324 2326 2328 2330 2332 2334 2336 2338 2340 2342 2344 2346 2348 2350 2352 2354 2356 2358 2360 2362 2364 2366 2368 2370 2372 2374 2376 2378 2380 2382 2384 2386 2388 2390 2392 2394 2396 2398 2400 2402 2404 2406 2408 2410 2412 2414 2416 2418 2420 2422 2424 2426 2428 2430 2432 2434 2436 2438 2440 2442 2444 2446 2448 2450 2452 2454 2456 2458 2460 2462 2464 2466 2468 2470 2472 2474 2476 2478 2480 2482 2484 2486 2488 2490 2492 2494 2496 2498 2500 2502 2504 2506 2508 2510 2512 2514 2516 2518 2520 2522 2524 2526 2528 2530 2532 2534 2536 2538 2540 2542 2544 2546 2548 2550 2552 2554 2556 2558 2560 2562 2564 2566 2568 2570 2572 2574 2576 2578 2580 2582 2584 2586 2588 2590 2592 2594 2596 2598 2600 2602 2604 2606 2608 2610 2612 2614 2616 2618 2620 2622 2624 2626 2628 2630 2632 2634 2636 2638 2640 2642 2644 2646 2648 2650 2652 2654 2656 2658 2660 2662 2664 2666 2668 2670 2672 2674 2676 2678 2680 2682 2684 2686 2688 2690 2692 2694 2696 2698 2700 2702 2704 2706 2708 2710 2712 2714 2716 2718 2720 2722 2724 2726 2728 2730 2732 2734 2736 2738 2740 2742 2744 2746 2748 2750 2752 2754 2756 2758 2760 2762 2764 2766 2768 2770 2772 2774 2776 2778 2780 2782 2784 2786 2788 2790 2792 2794 2796 2798 2800 2802 2804 2806 2808 2810 2812 2814 2816 2818 2820 2822 2824 2826 2828 2830 2832 2834 2836 2838 2840 2842 2844 2846 2848 2850 2852 2854 2856 2858 2860 2862 2864 2866 2868 2870 2872 2874 2876 2878 2880 2882 2884 2886 2888 2890 2892 2894 2896 2898 2900 2902 2904 2906 2908 2910 2912 2914 2916 2918 2920 2922 2924 2926 2928 2930 2932 2934 2936 2938 2940 2942 2944 2946 2948 2950 2952 2954 2956 2958 2960 2962 2964 2966 2968 2970 2972 2974 2976 2978 2980 2982 2984 2986 2988 2990 2992 2994 2996 2998 3000 3002 3004 3006 3008 3010 3012 3014 3016 3018 3020 3022 3024 3026 3028 3030 3032 3034 3036 3038 3040 3042 3044 3046 3048 3050 3052 3054 3056 3058 3060 3062 3064 3066 3068 3070 3072 3074 3076 3078 3080 3082 3084 3086 3088 3090 3092 3094 3096 3098 3100 3102 3104 3106 3108 3110 3112 3114 3116 3118 3120 3122 3124 3126 3128 3130 3132 3134 3136 3138 3140 3142 3144 3146 3148 3150 3152 3154 3156 3158 3160 3162 3164 3166 3168 3170 3172 3174 3176 3178 3180 3182 3184 3186 3188 3190 3192 3194 3196 3198 3200 3202 3204 3206 3208 3210 3212 3214 3216 3218 3220 3222 3224 3226 3228 3230 3232 3234 3236 3238 3240 3242 3244 3246 3248 3250 3252 3254 3256 3258 3260 3262 3264 3266 3268 3270 3272 3274 3276 3278 3280 3282 3284 3286 3288 3290 3292 3294 3296 3298 3300 3302 3304 3306 3308 3310 3312 3314 33

FIG. 20



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 Dkt. No. 1875.138000G; Group Art Unit: To Be Assigned
 Inventors: Arya R. Behzad; Tel.: (202) 371-2600
 Title: Large Gain Range, High Linearity, Low Noise MOS
 VGA

FIG. 21

PPL Xtdl REFERENCE=10MHz
 LO-1, 10MHz FREQUENCY STEPS
 LO-2, 100kHz FREQUENCY STEPS

44MHz IF

NOTE
 •LO-2 REF=100KHz,
 SO DIVIDE RANGE=9216 TO 9280

TABLE OF FREQUENCIES BASED ON
 COARSE/FINE PLL SOLUTION:

Fr1 (MHz)	50	56	62	68	74	80	86	92	98	104	110	116	122	128	"	854	860
LO-1(MHz)	1250	1260	1260	1270	1270	1280	1290	1290	1300	1300	1310	1320	1320	1330	"	2050	2060
IF-1 (MHz)	1200	1204	1198	1202	1196	1200	1204	1198	1202	1196	1200	1204	1198	1202	"	1196	1200
LO-2(MHz)	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	"	921.6	924.8
IF-2(MHz)	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	"	274.4	275.2
LO-3(MHz)	231.2	232	230.8	232	230	231	232	231	232	230	231	232	231	232	"	230	231
IF-3(MHz)	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	"	44.0	44.0

2102

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 VGA

FIG. 22

36MHz IF

PPL Xtol REFERENCE=10MHz
 LO-1, 10MHz FREQUENCY STEPS
 LO-2, 100kHz FREQUENCY STEPS

NOTE

• LO-2 REF=100KHz.
 SO DIVIDE RANGE=9280 TO 9340

TABLE OF FREQUENCIES BASED ON
 COARSE/FINE PLL SOLUTION:

Frf (MHz)	50	58	66	74	82	90	98	106	114	122	130	138	146	154	"	852	860
LO-1(MHz)	1250	1260	1270	1270	1280	1290	1300	1310	1310	1320	1330	1340	1350	1350	"	2050	2060
IF-1 (MHz)	1200	1202	1204	1196	1198	1200	1202	1204	1196	1198	1200	1202	1204	1196	"	1198	1200
LO-2(MHz)	931.2	932.8	934.4	928.0	930	931	933	934	928.0	930	931	933	934	928.0	"	929.60	931.2
IF-2(MHz)	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	"	268.4	268.8
LO-3(MHz)	232.8	233.2	233.6	232	232	233	233	234	232	232	233	233	234	232.0	"	232.4	232.8
IF-3(MHz)	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	"	36.0	36.0

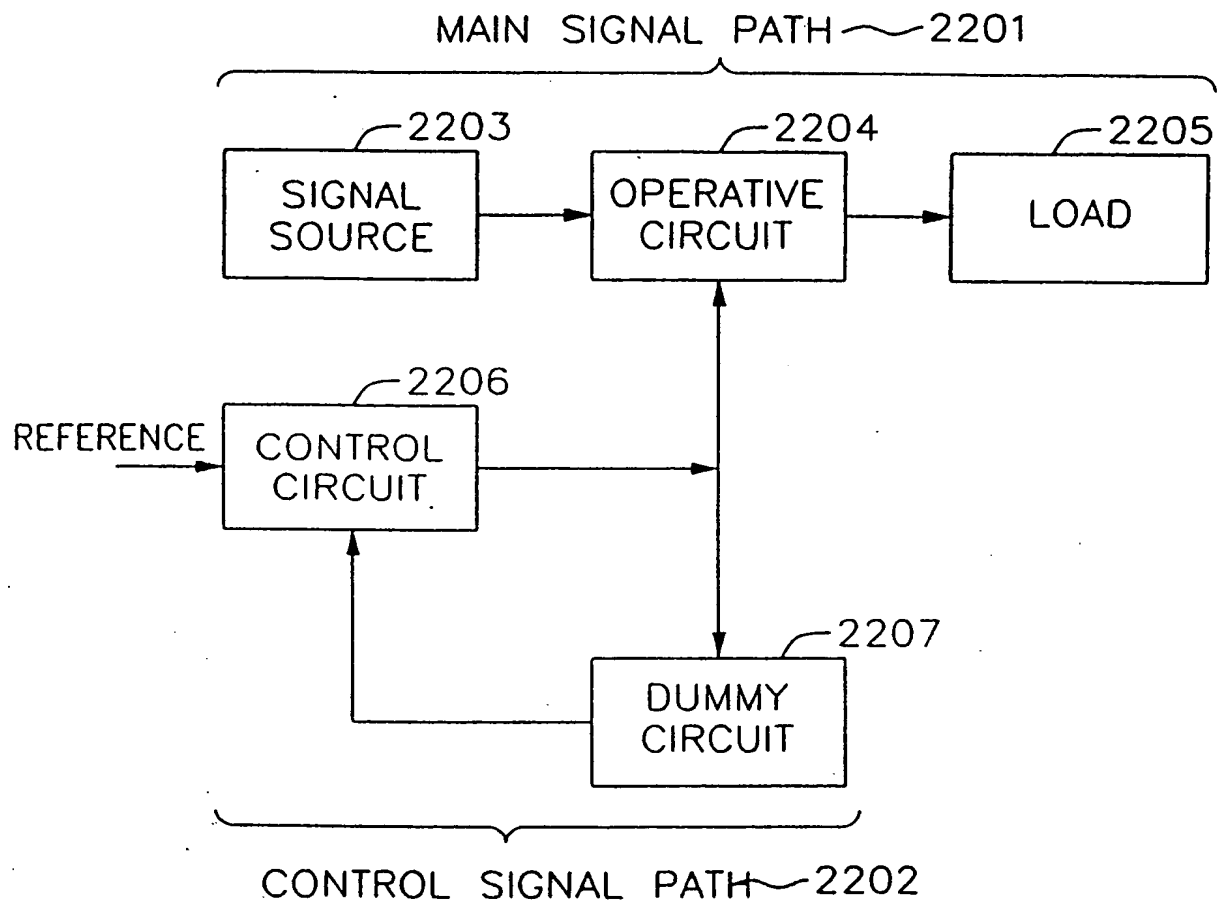
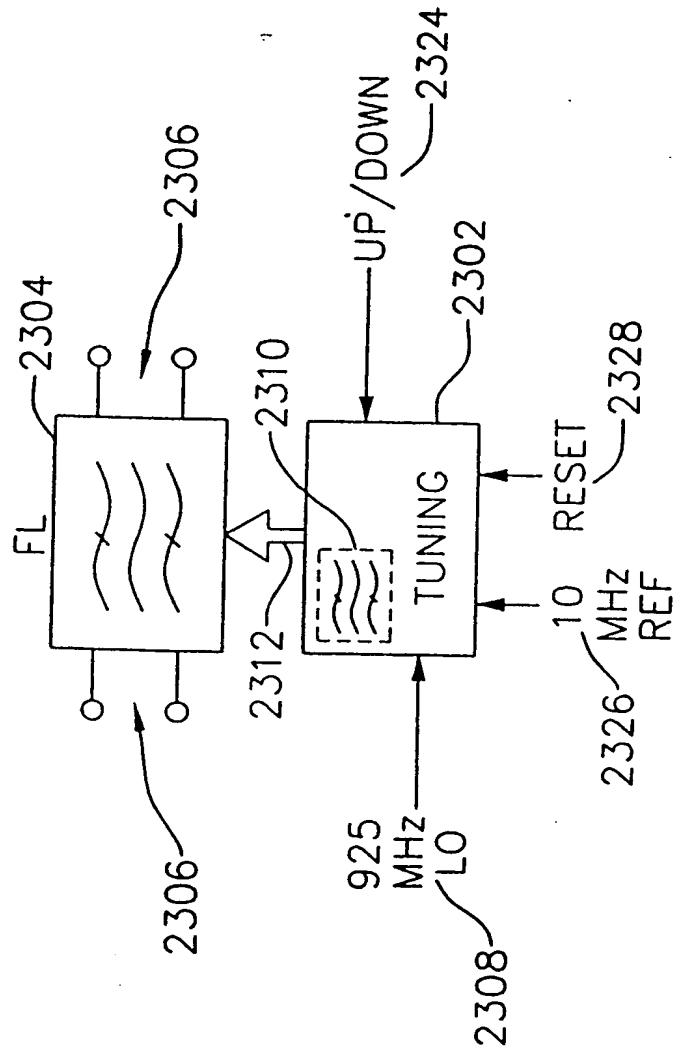
FIG. 23

FIG. 24a




```

graph TD
    2312[POWER UP] --> 2314[PLL LOCK]
    2314 --> 2316([START TUNING PROCEDURE])
    2316 --> 2320[TUNE DUMMY FILTER TO A FIXED FREQUENCY]
    2320 --> 2318[APPLY COMPONENT SCALING VALUES TO CENTER THE ACTUAL FILTER RESPONSE]
    2318 --> 2322[TUNING SWITCHES OFF TO ELIMINATE NOISE PATH]
    2322 --> 2324{IS FILTER CENTERED?}
    2324 -- YES --> 2326[INTRODUCE TUNING OFFSET]
    2324 -- NO --> 2328[SWITCH IN MORE CAPACITANCE]
    2328 --> 2320
    2326 --> 2330{TUNING OFFSET DESIRED?}
    2330 -- YES --> 2332[INTRODUCE TUNING OFFSET]
    2330 -- NO --> 2334([END])
    2332 --> 2326
    2326 --> 2336([END])

```

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 Inventors: Arya R. Behzad; Tel.: (202) 371-2600
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 VGA

FIG. 24c

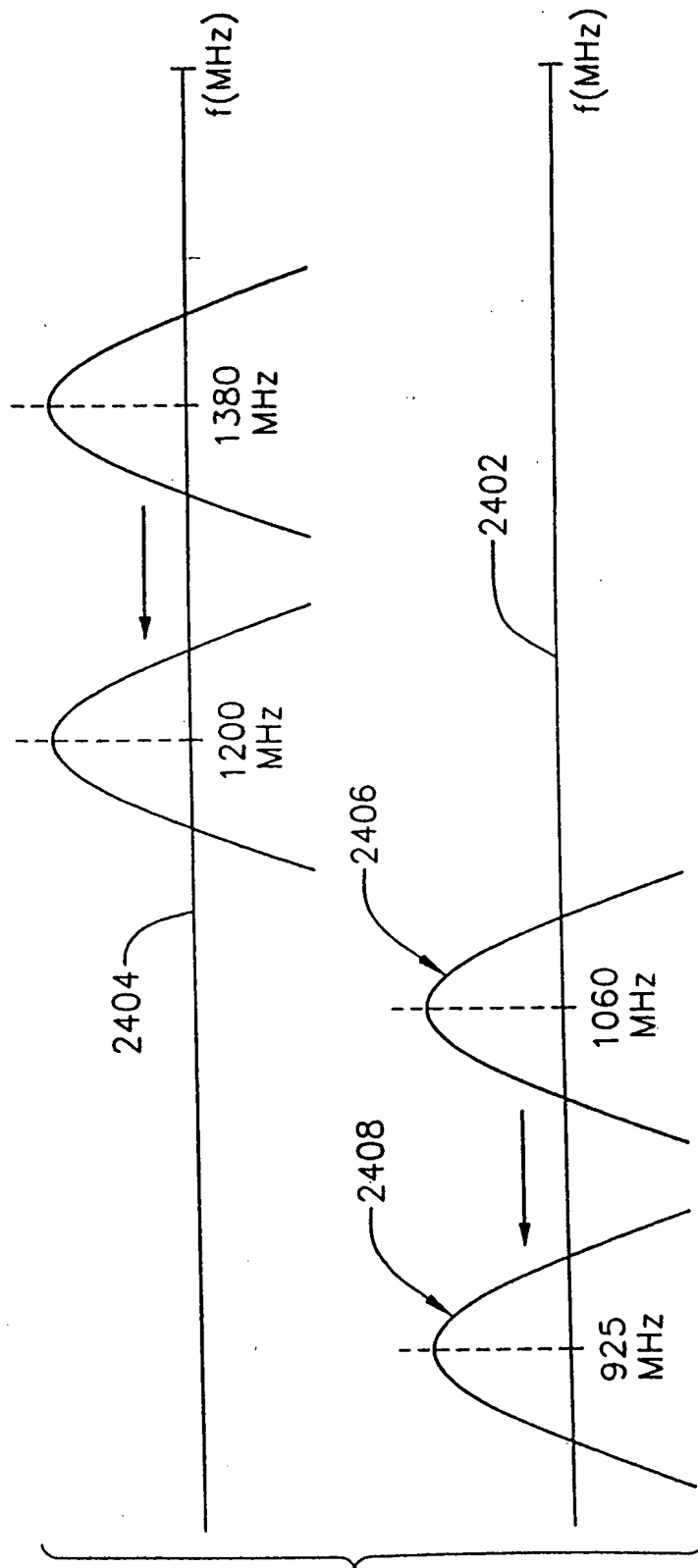


FIG. 25

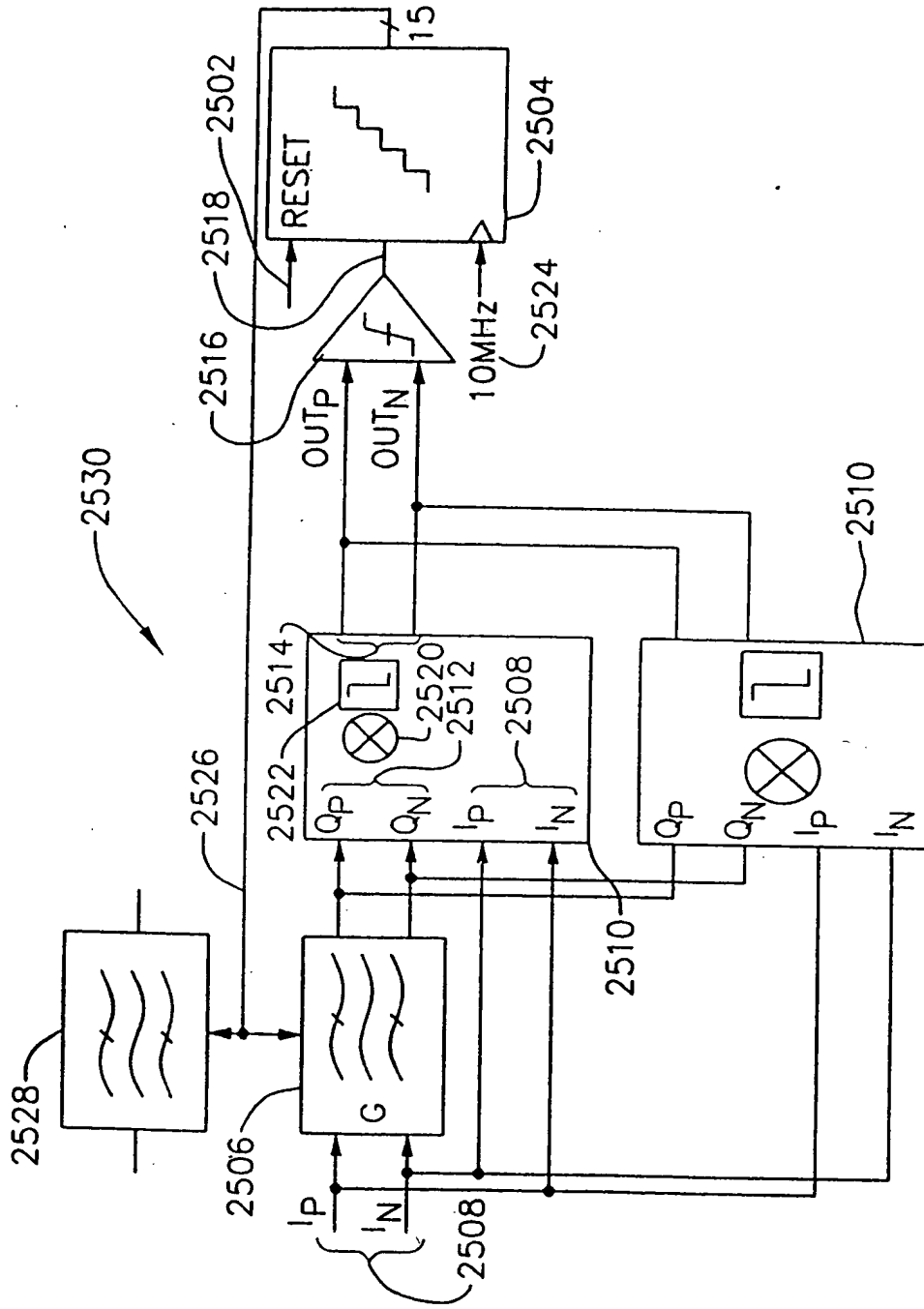
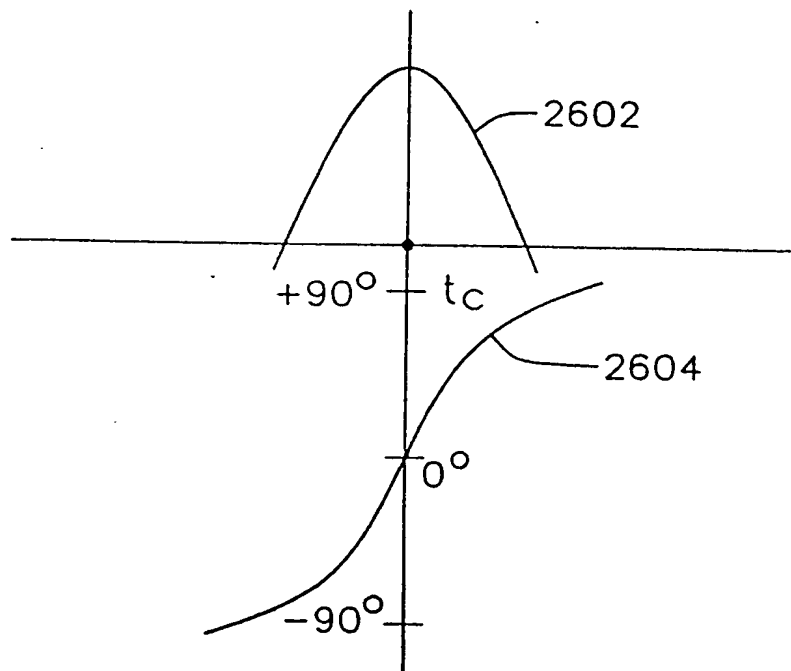


FIG. 26

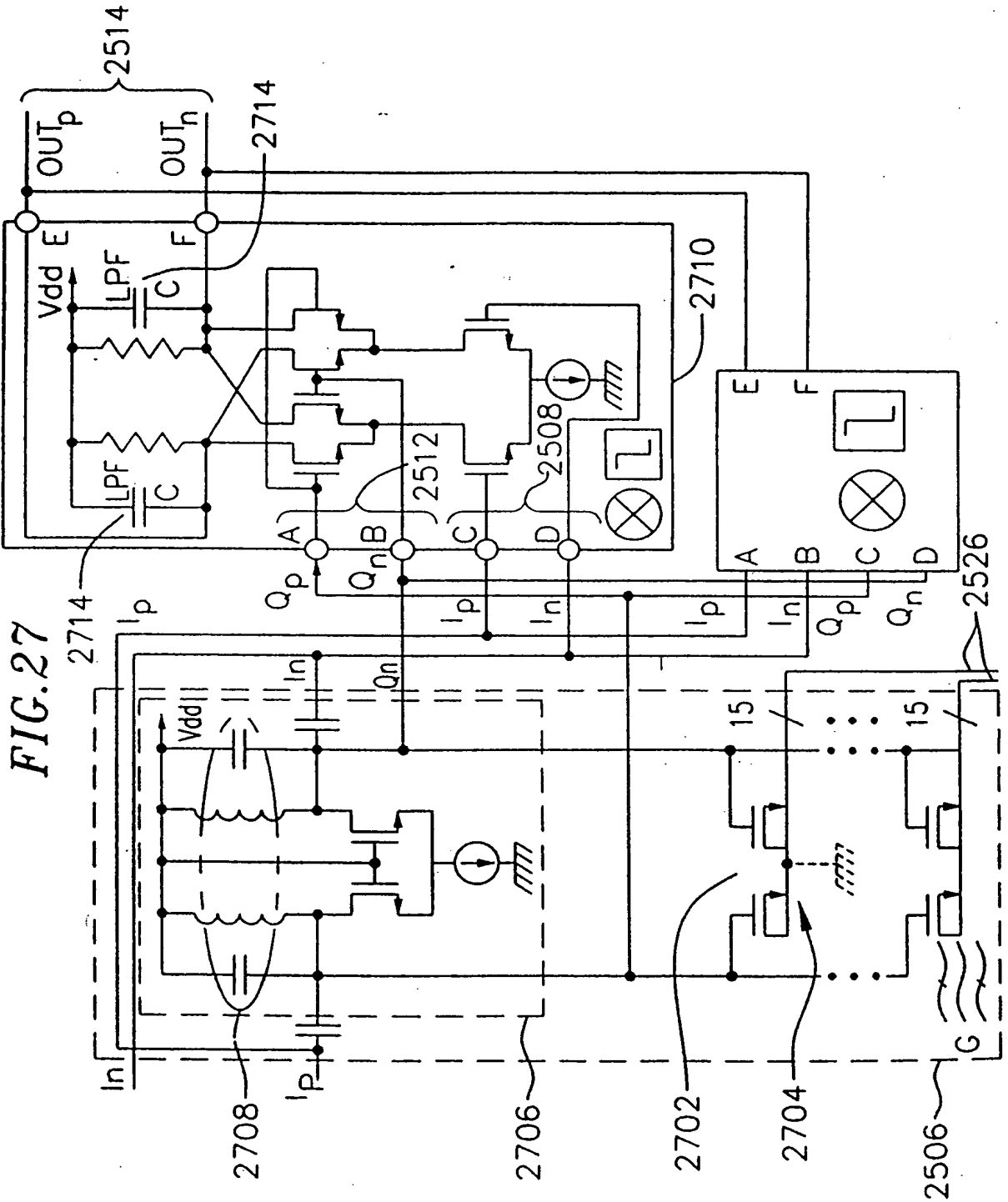


FIG. 28a

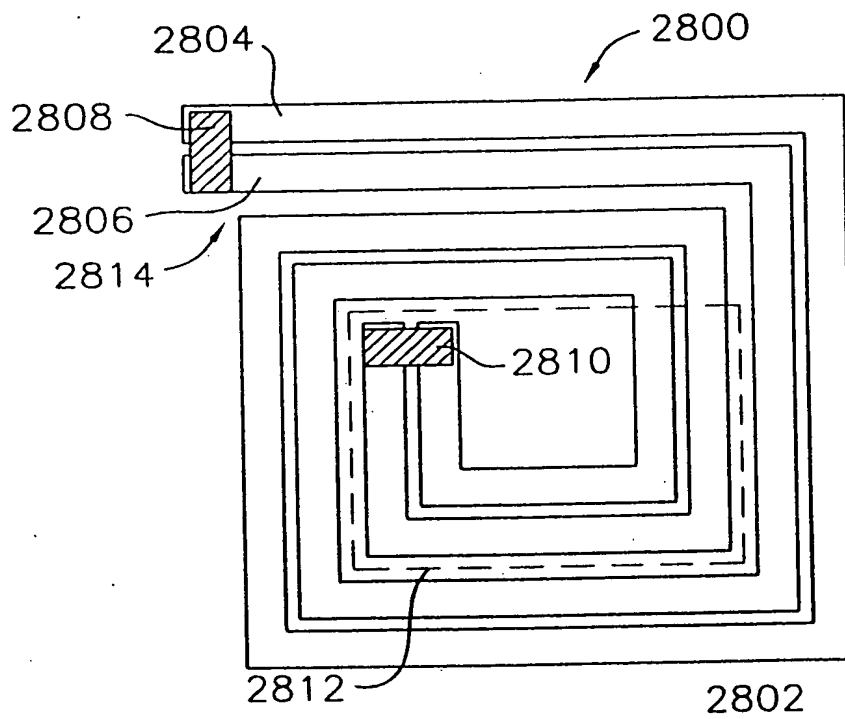


FIG. 28b

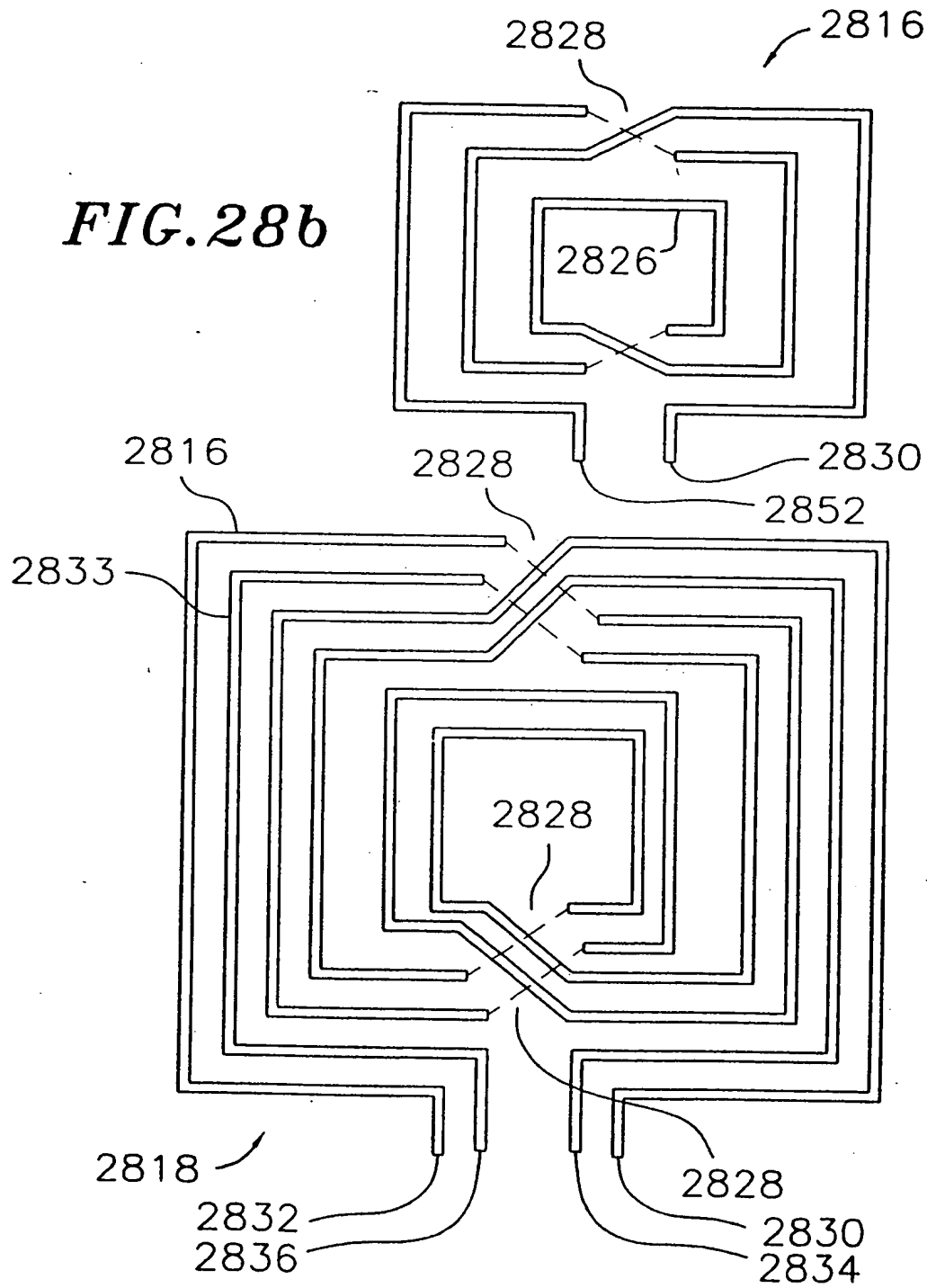


FIG. 28c

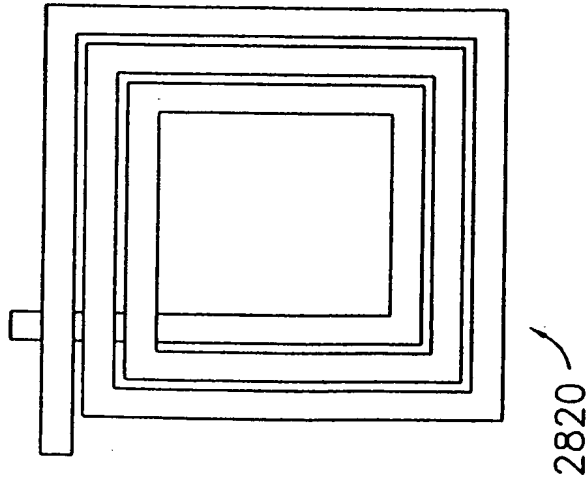


FIG. 28d

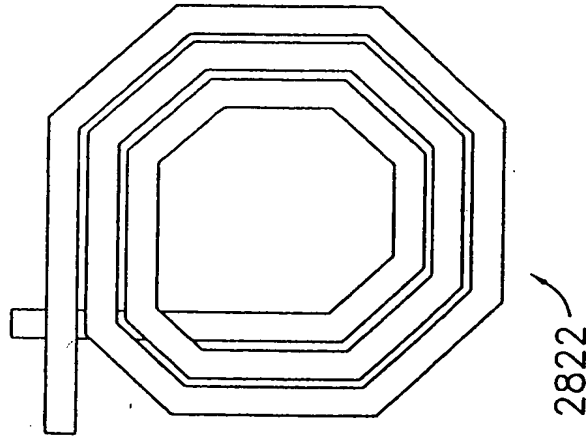


FIG. 28e

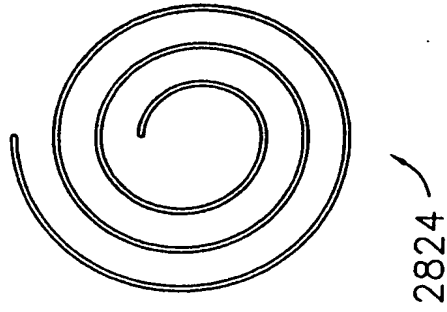


FIG.28f

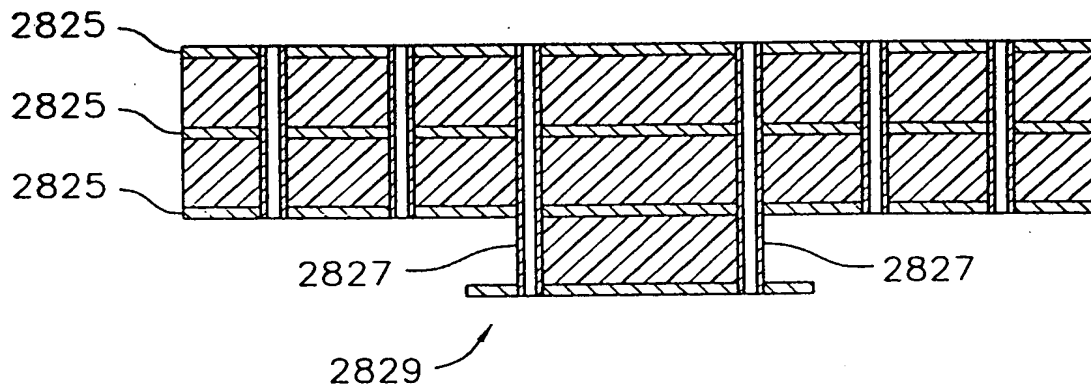
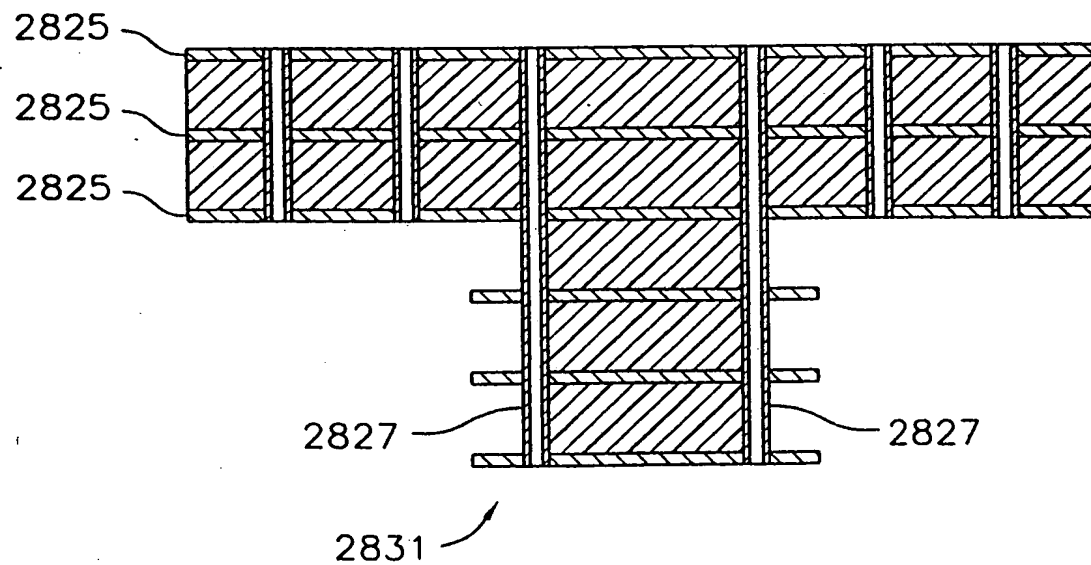
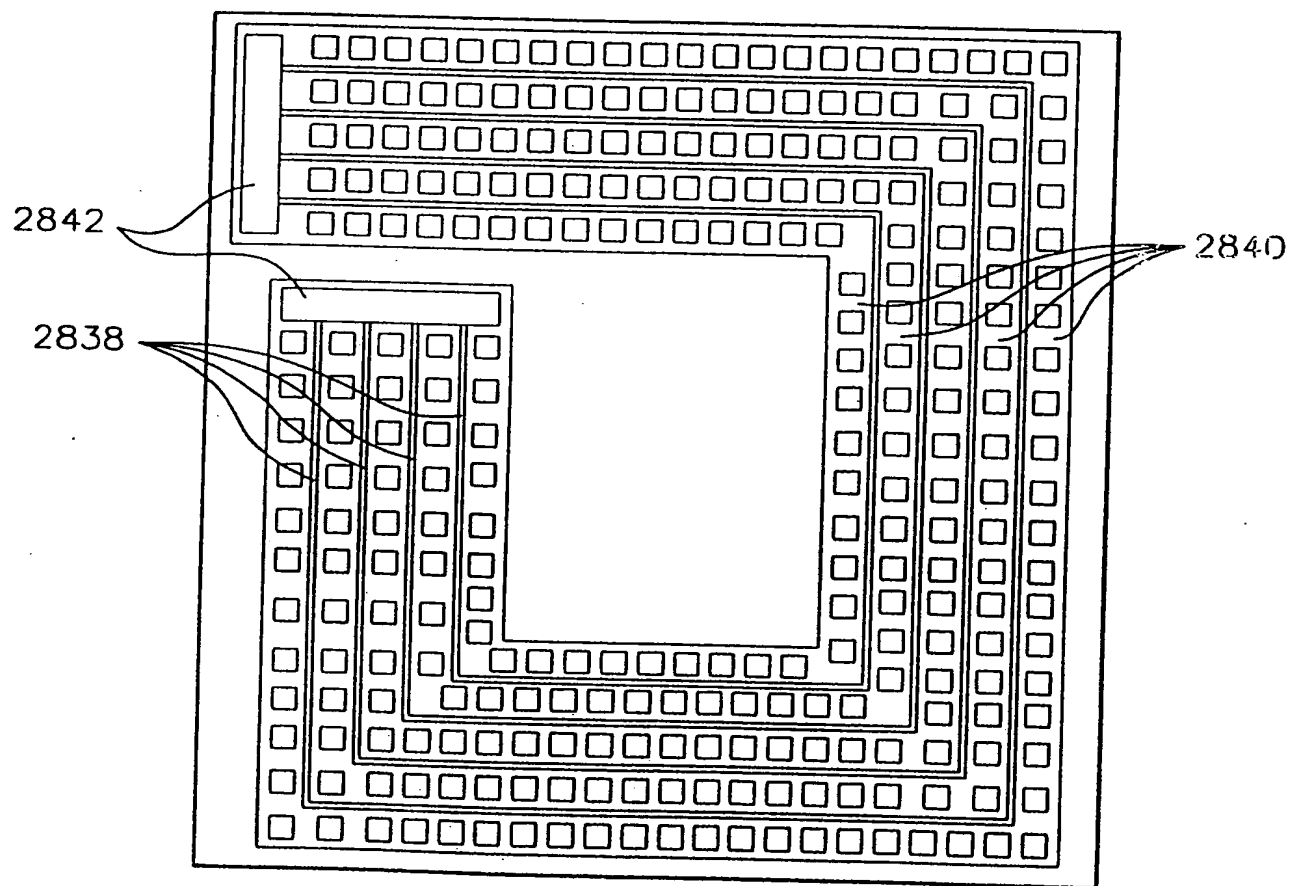


FIG.28g

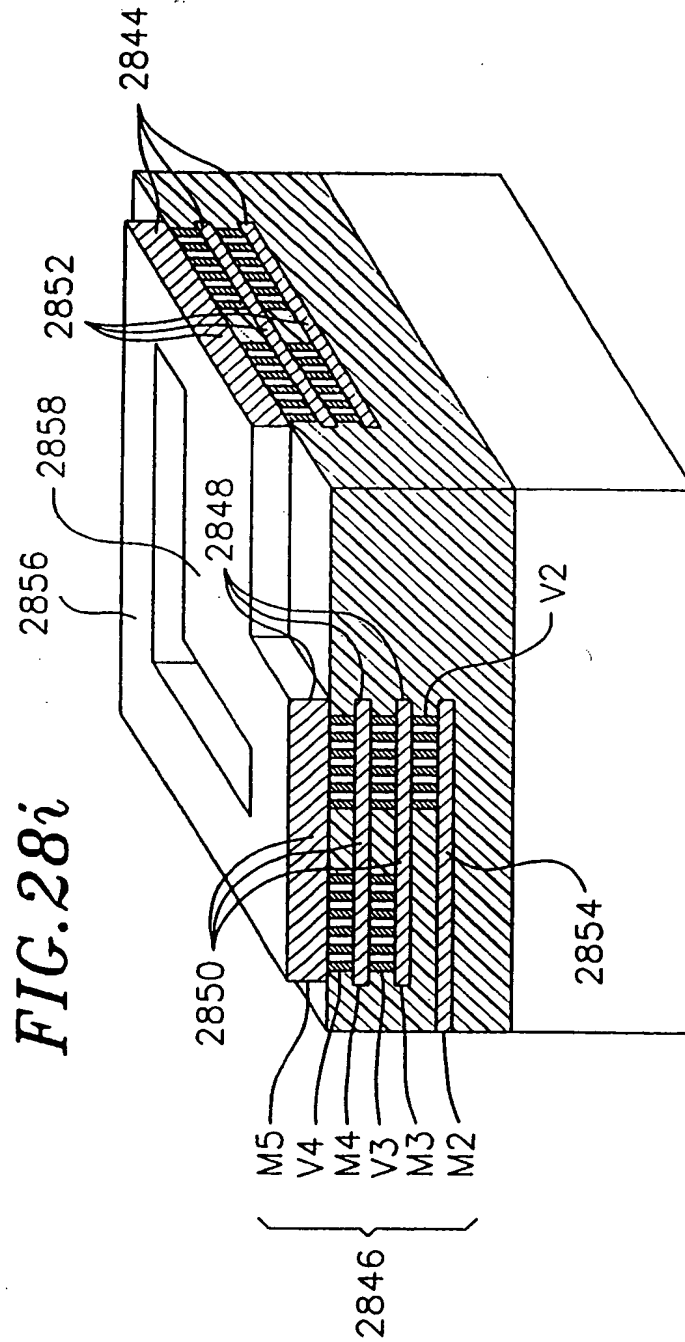


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 Inventors: Arya R. Behzad; Tel.: (202) 371-2600
 Title: Large Gain Range, High Linearity, Low Noise MOS
 VGA

FIG.28h

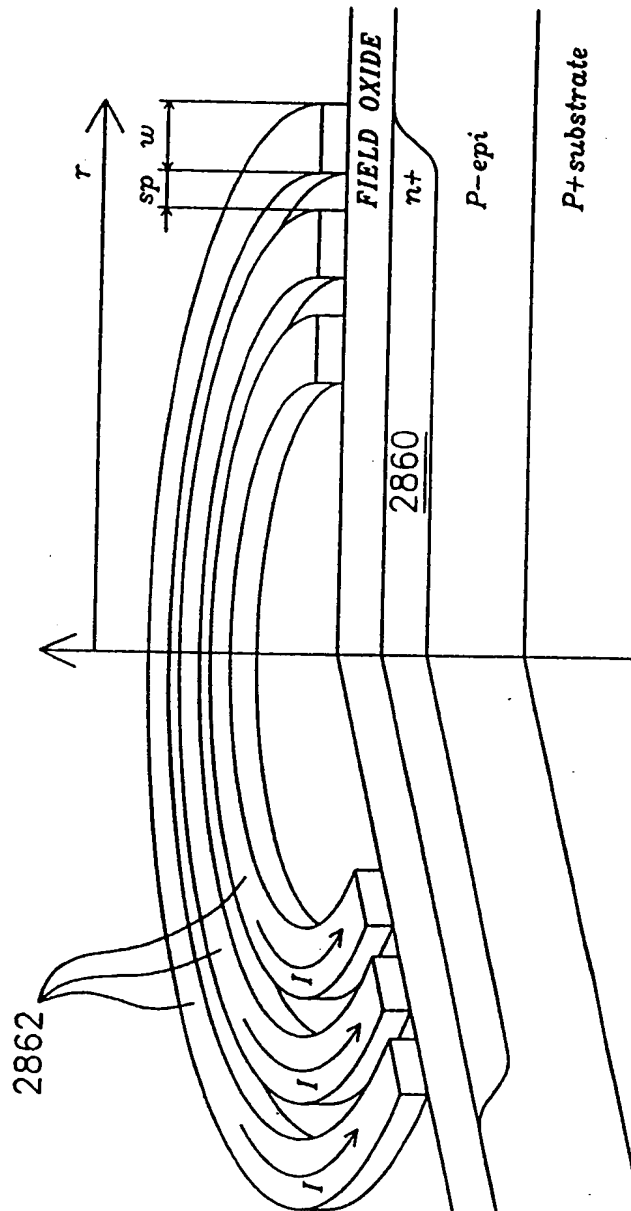


Appl. No. *To Be Assigned*; Filed: *Herewith*
 Dkt. No. 1875.138000G; Group Art Unit: *To Be Assigned*
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 Title: Large Gain Range, High Linearity, Low Noise MOS
 VGA



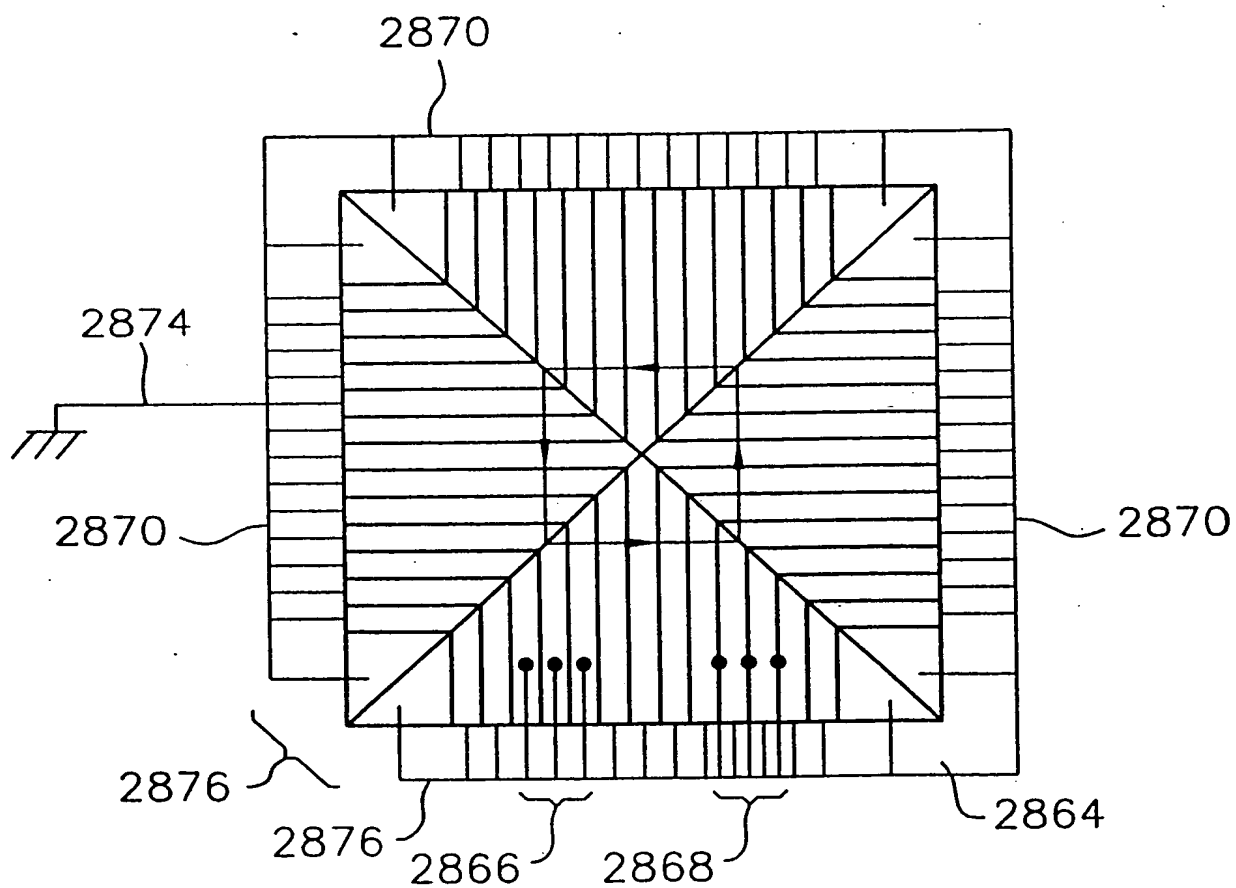
Appl. No. *To Be Assigned*; Filed: *Herewith*
 Dkt. No. 1875.138000G; Group Art Unit: *To Be Assigned*
 Inventors: Arya R. Behzad; Tel.: (202) 371-2600
 Title: Large Gain Range, High Linearity, Low Noise MOS
 VGA

FIG. 28j



Appl. No. *To Be Assigned*; Filed: *Herewith*
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 Inventors: Arya R. Behzad; Tel.: (202) 371-2600
 Title: Large Gain Range, High Linearity, Low Noise MOS
 VGA

FIG. 28k



Appl. No. *To Be Assigned*; Filed: *Herewith*
Dkt. No. 1875.138000G; Group Art Unit: *To Be Assigned*
Inventors: Arya R. Behzad; Tel.: (202) 371-2600
Title: Large Gain Range, High Linearity, Low Noise MOS
VGA

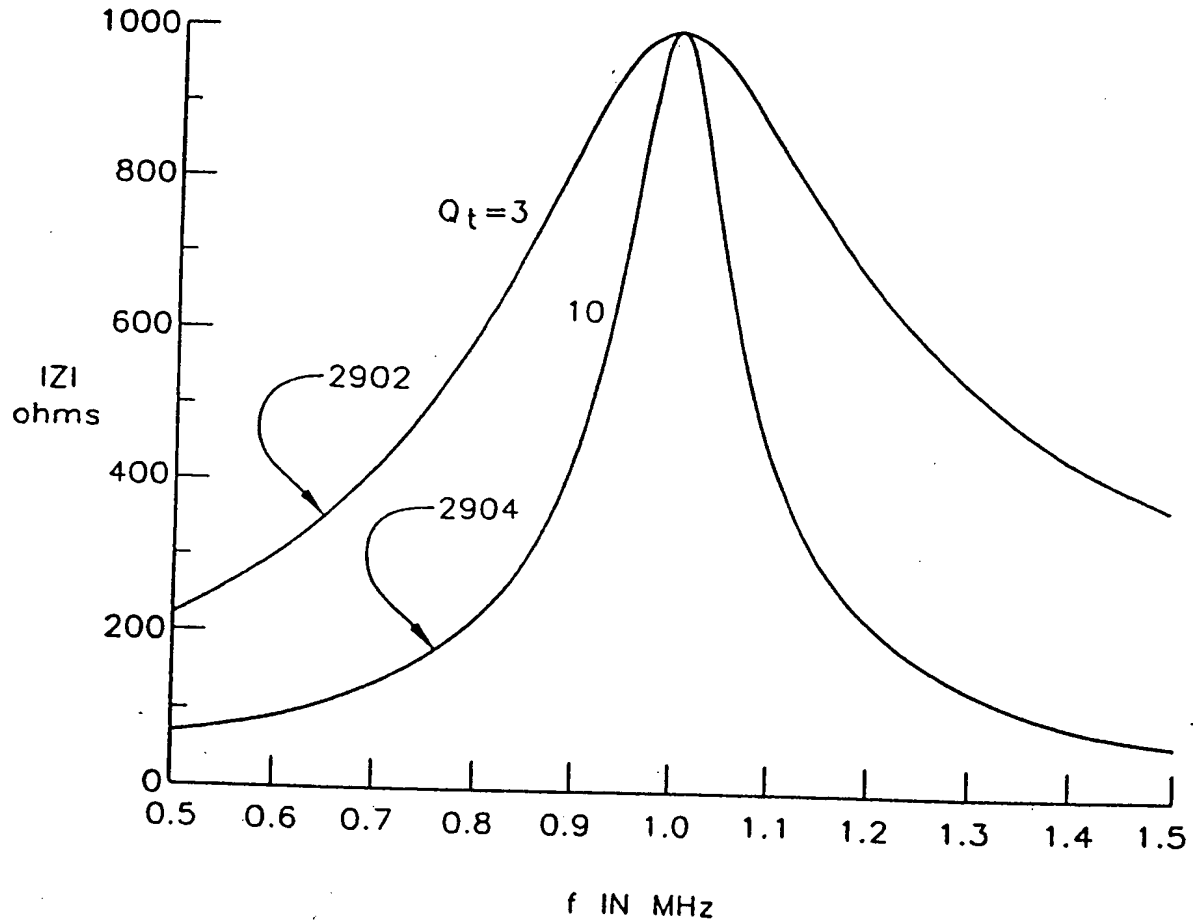
FIG. 29

FIG. 30

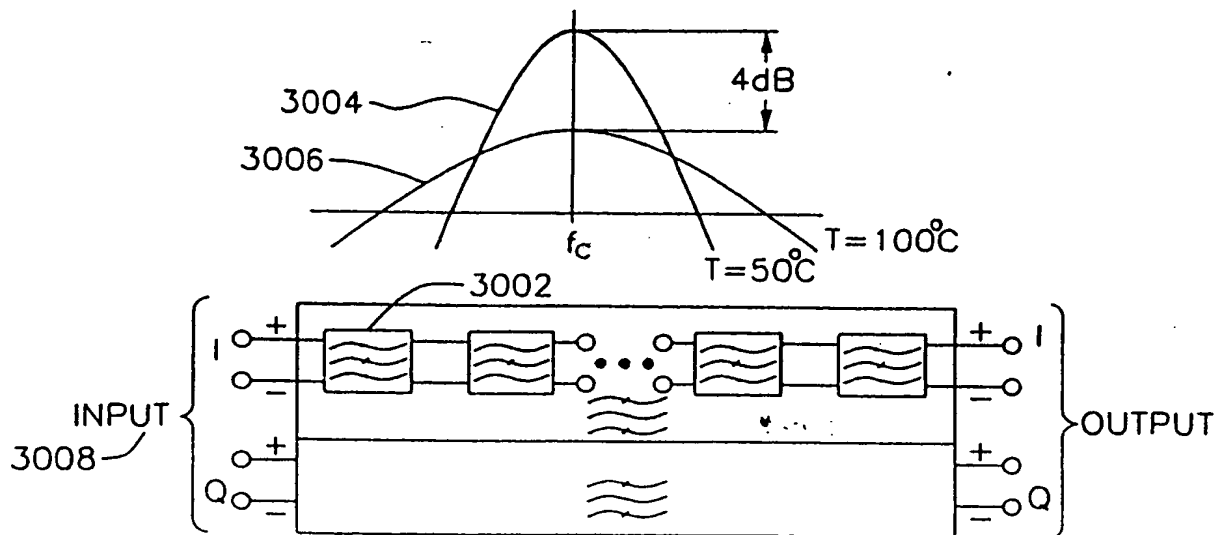


FIG. 31

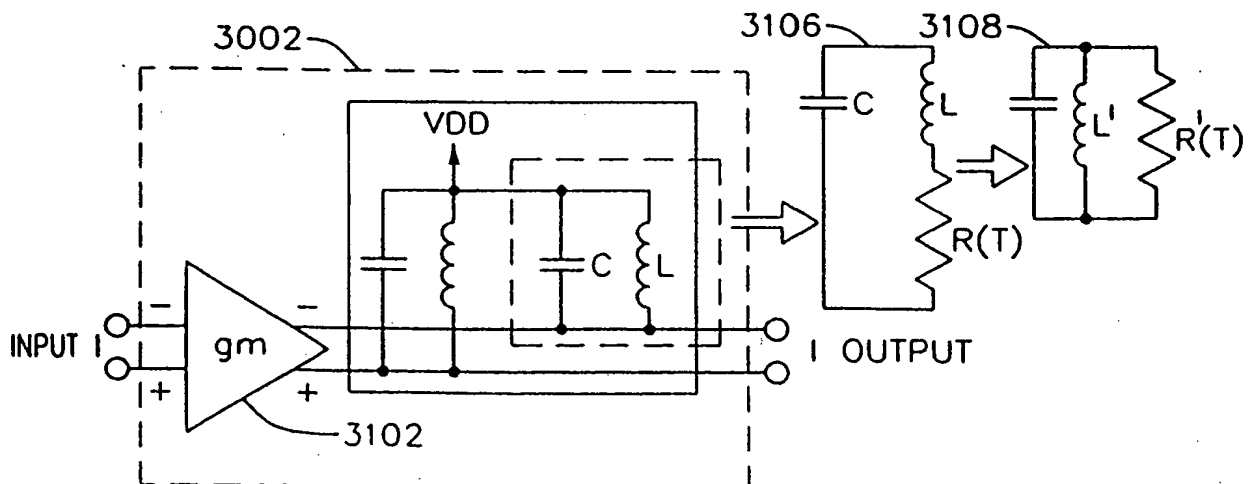


FIG. 32

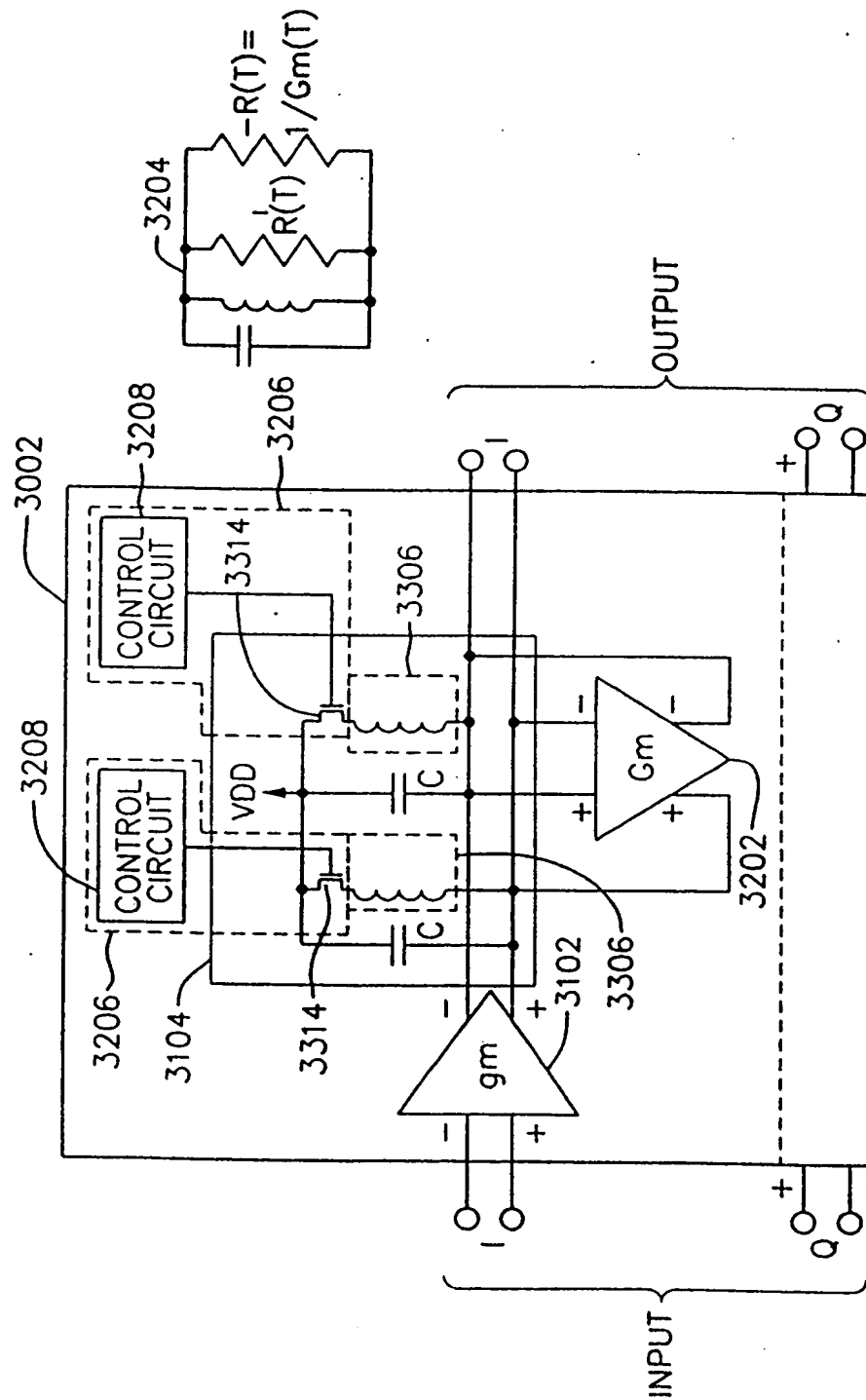
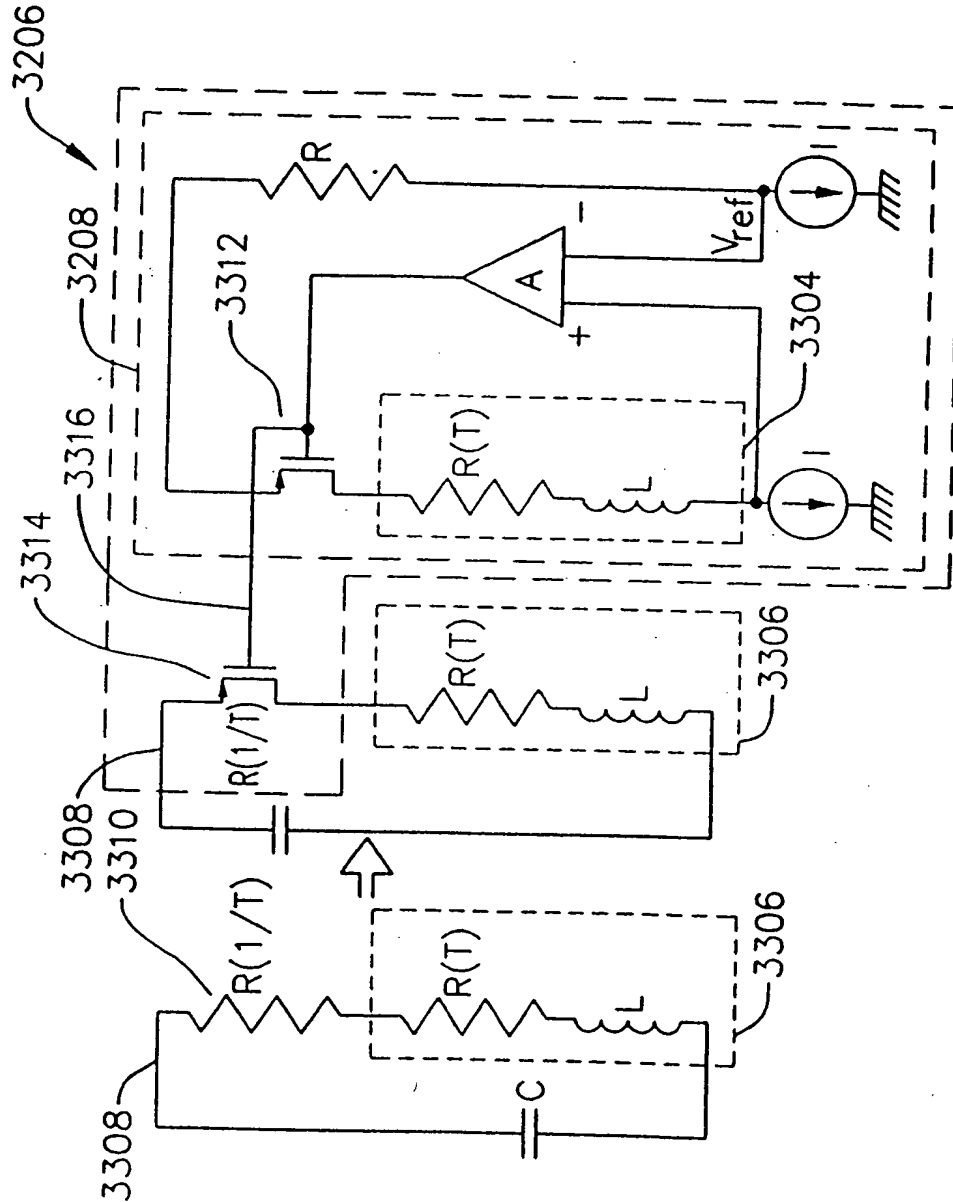


FIG. 33



Appl. No. To Be Assigned; Filed: Herewith
 Dkt. No. 1875.138000G; Group Art Unit: To Be Assigned
 Inventors: Arya R. Behzad; Tel.: (202) 371-2600
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 VGA

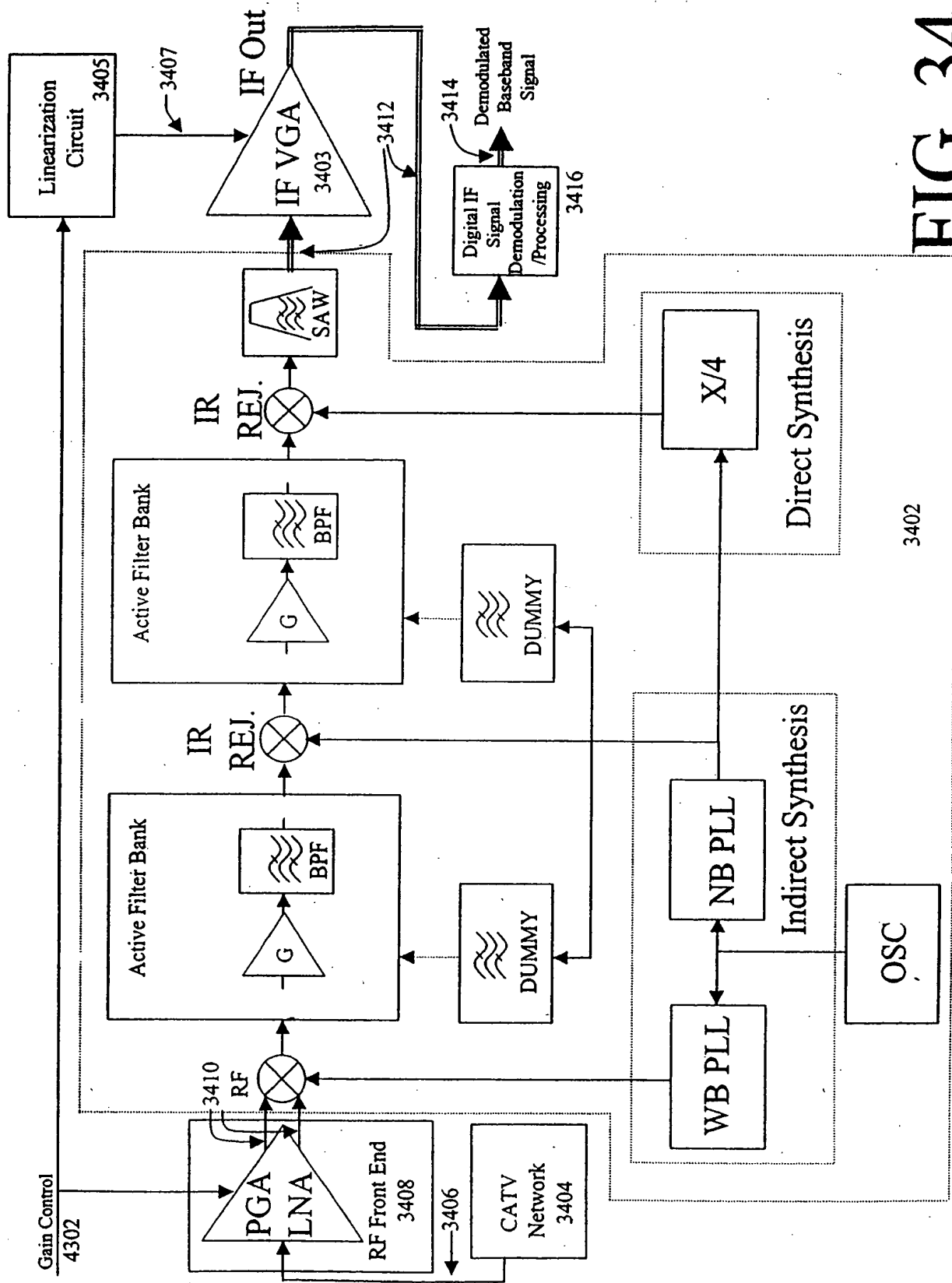


FIG. 34

Appl. No. *To Be Assigned*; Filed: *Herewith*
Dkt. No. 1875.138000G; Group Art Unit: *To Be Assigned*
Inventors: Arya R. Behzad; Tel.: (202) 371-2600
Title: Large Gain Range, High Linearity, Low Noise MOS
VGA

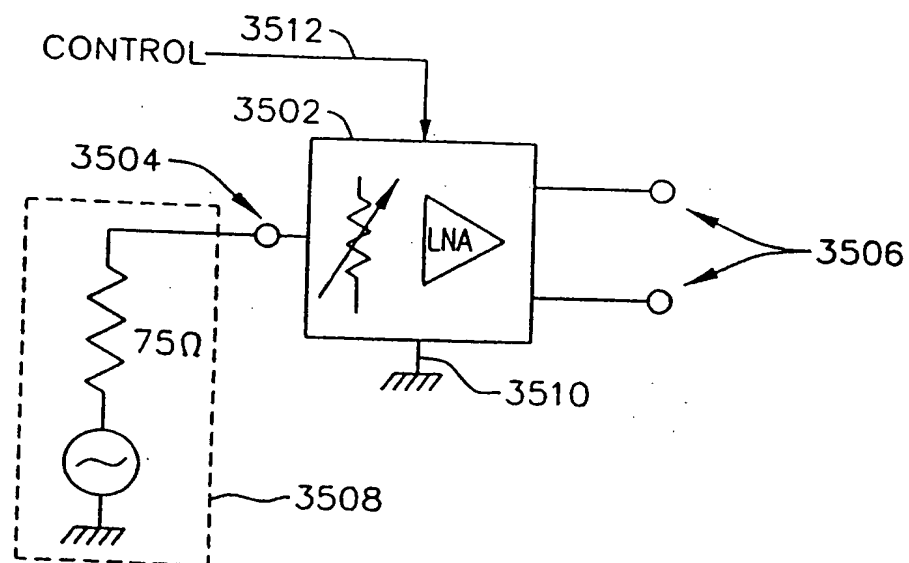
FIG. 35

FIG. 37

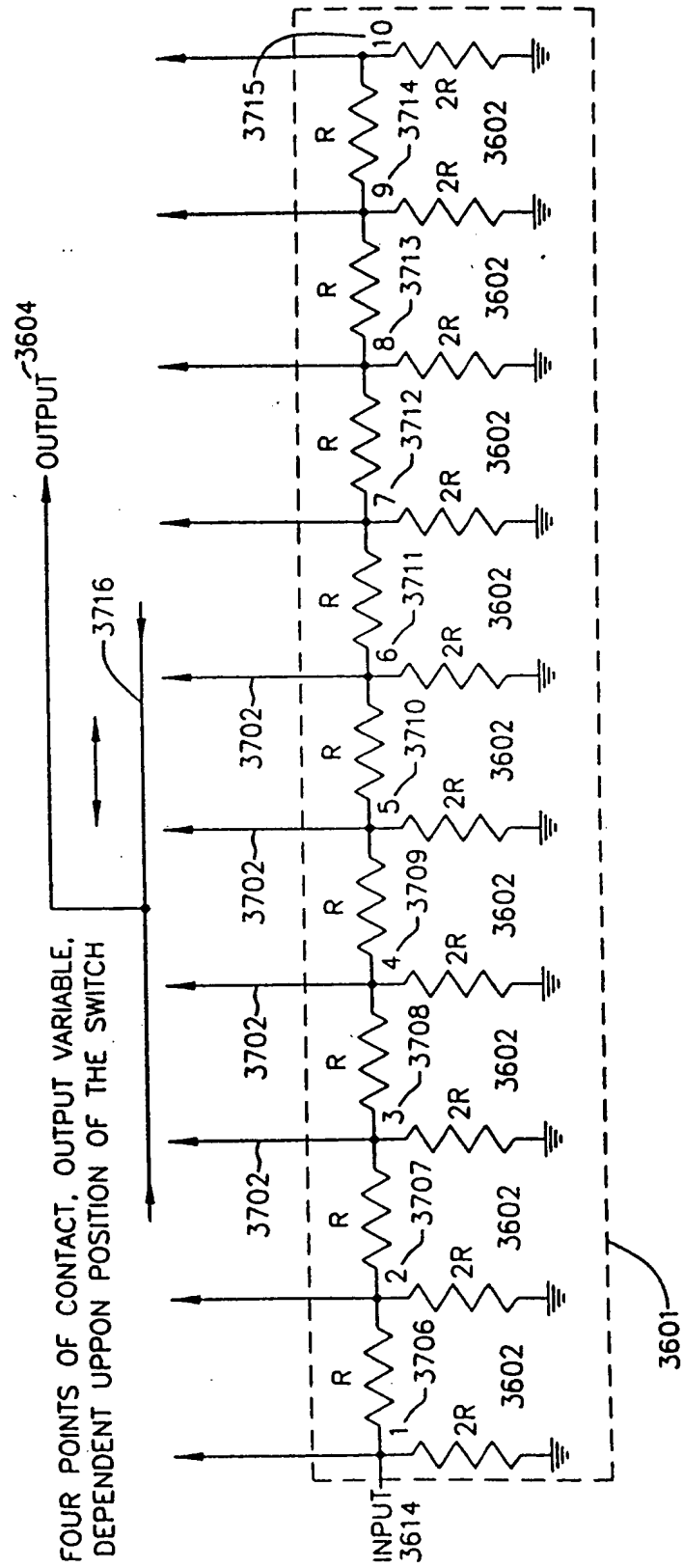


FIG. 38

PGA SETTINGS

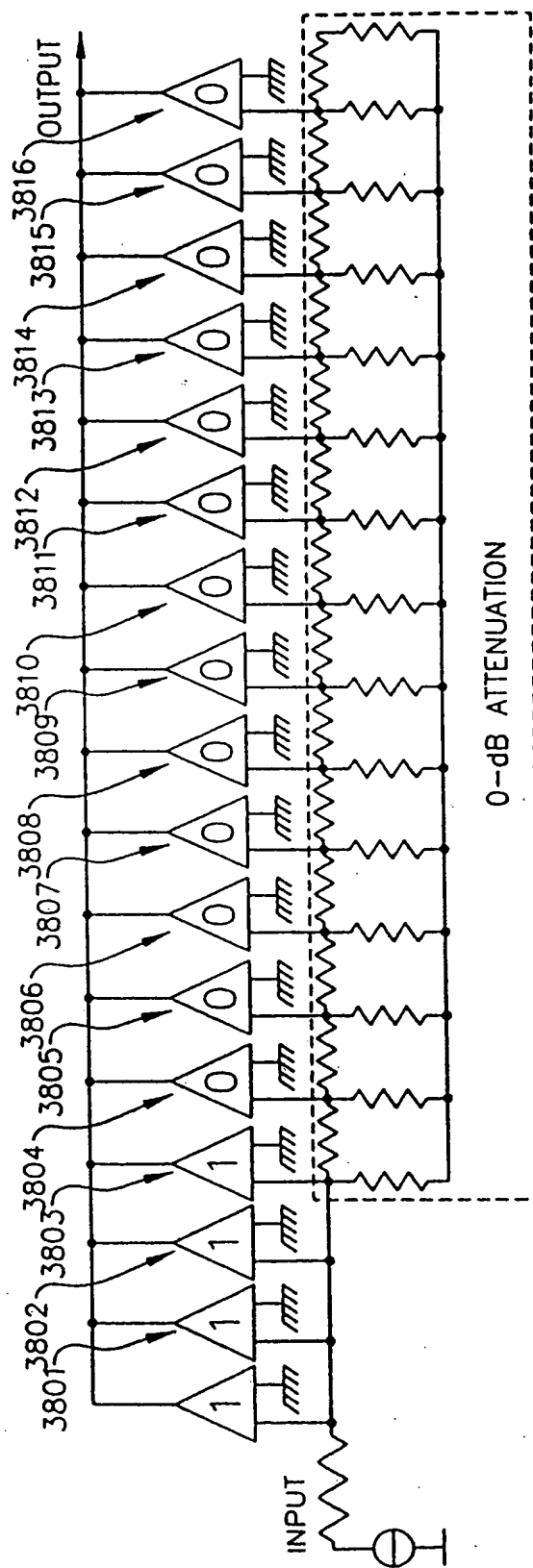


FIG. 39

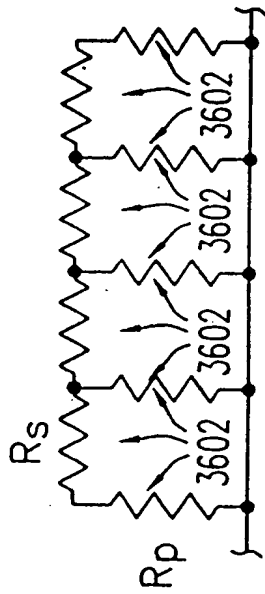
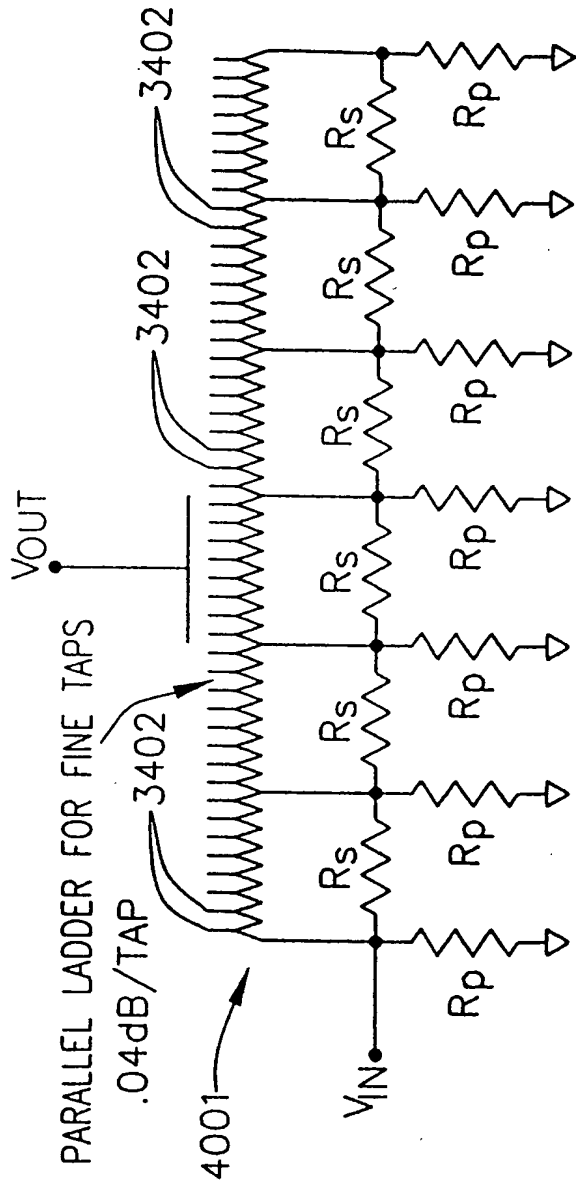


FIG. 40

PGA ARCHITECTURE



The diagram illustrates a resistive divider circuit. It consists of 10 parallel stages connected in series. Each stage contains 10 resistors in parallel, labeled R_s . The output of each stage is taken from a common point, and the total output is taken from the final stage. The output is connected to a load resistor R_p . The input is labeled "INPUT" and the output is labeled "OUTPUT". The circuit is labeled "RESISTIVE DIVIDER".

Labels in the diagram include:

- RESISTIVE DIVIDER
- INPUT
- OUTPUT
- 0dB R_s
- 1dB R_s
- 2dB R_s
- 3dB R_s
- 4dB R_s
- 10 IN PARALLEL
- EACH RESISTOR: 130 Ohm
- 10 IN SERIES
- R_p

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 VGA

FIG. 42

NON-MONOTONICITY

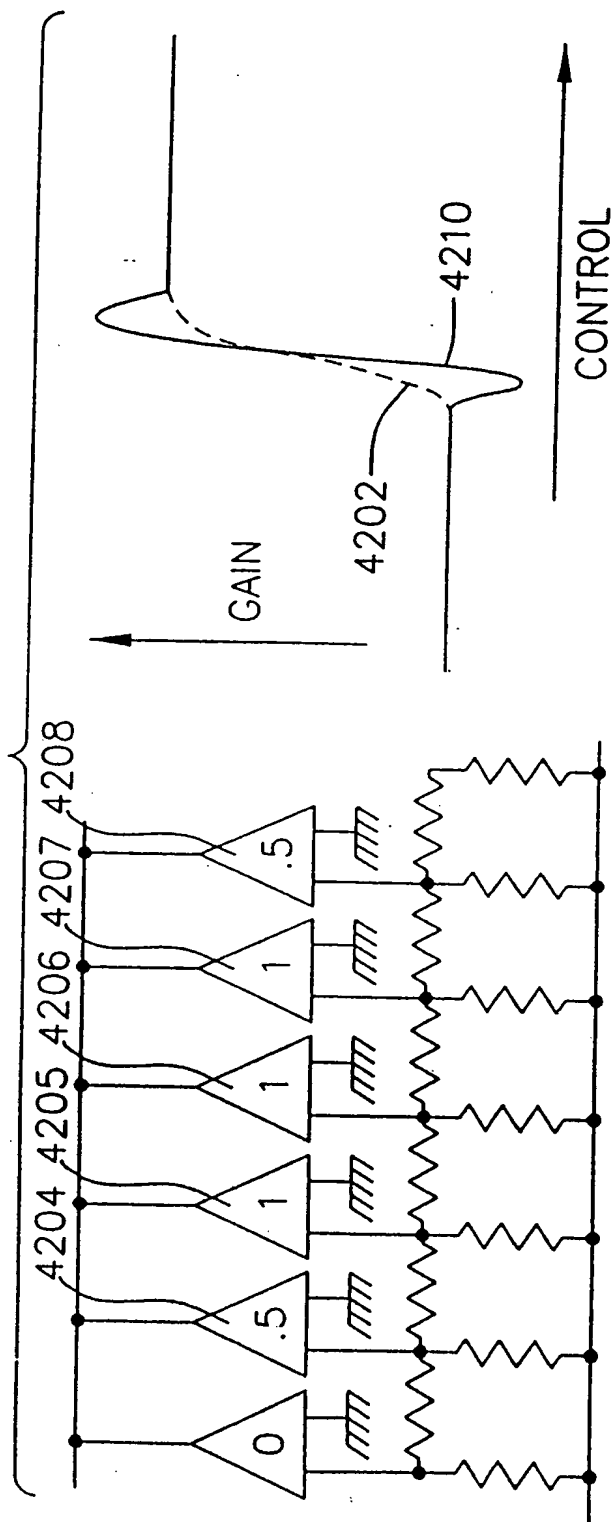
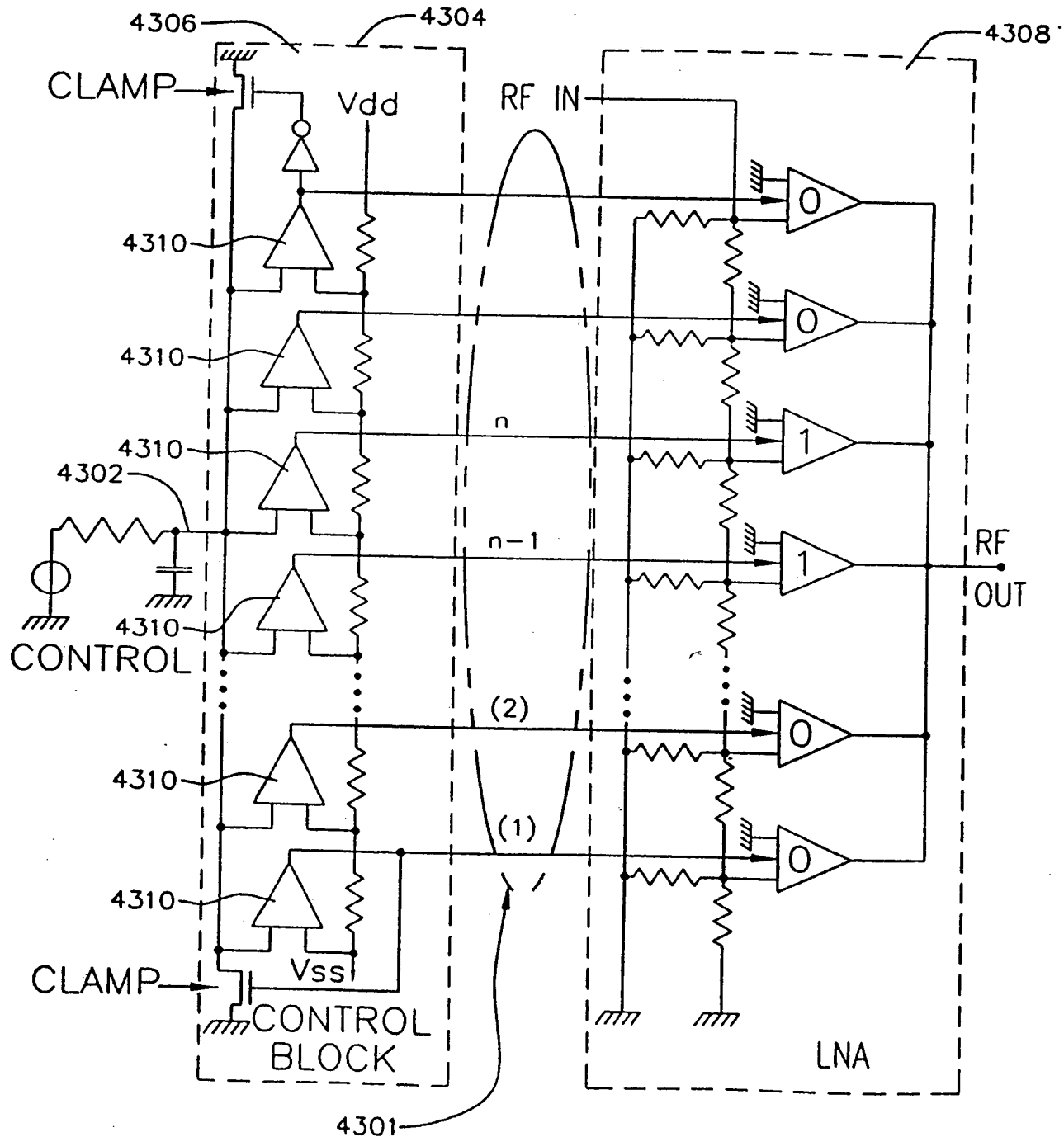


FIG. 43
 CLAMPING CONTROL RANGE



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FIG. 44a
 CONTROLLED GAIN COMPARATOR

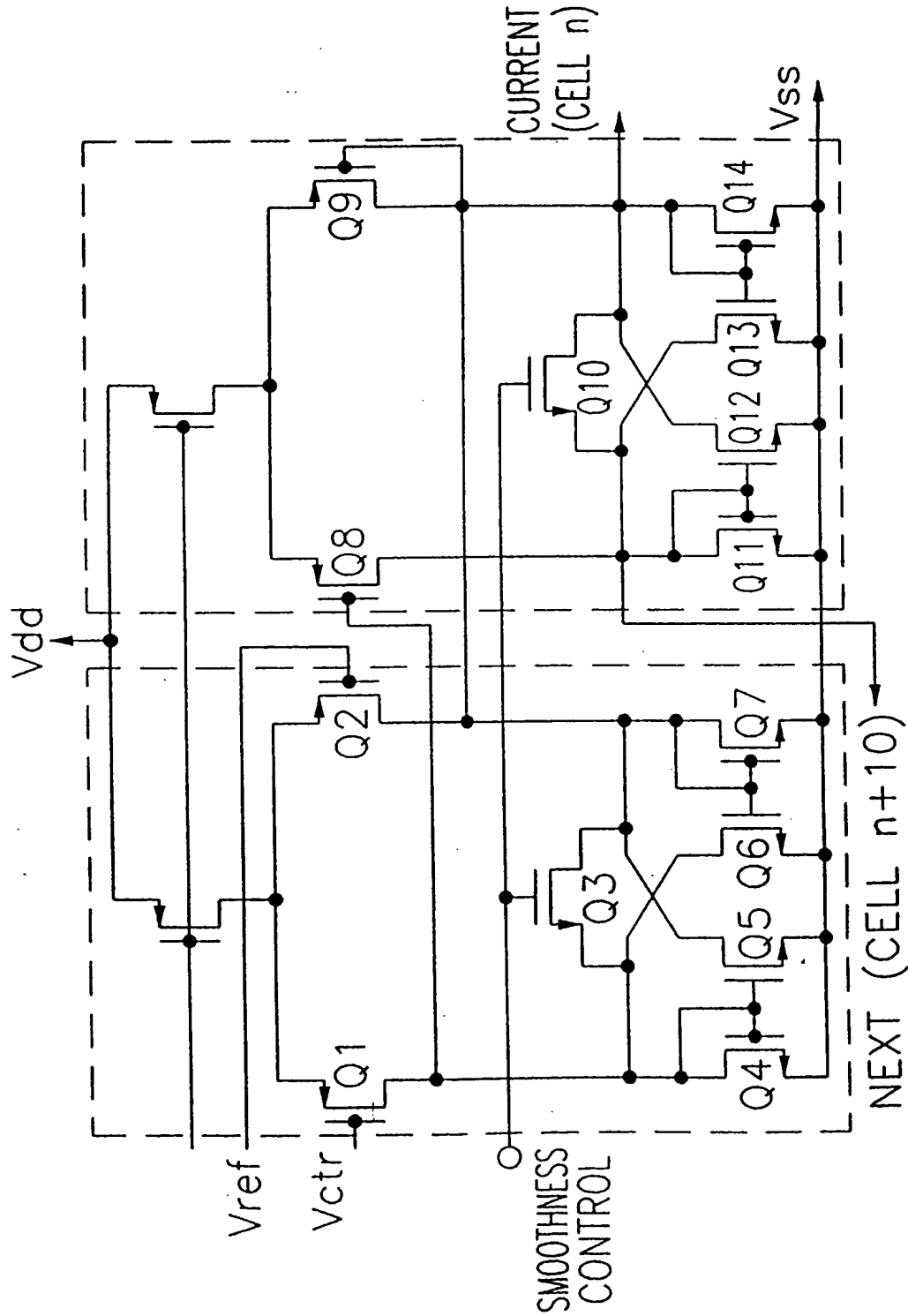


FIG. 44b

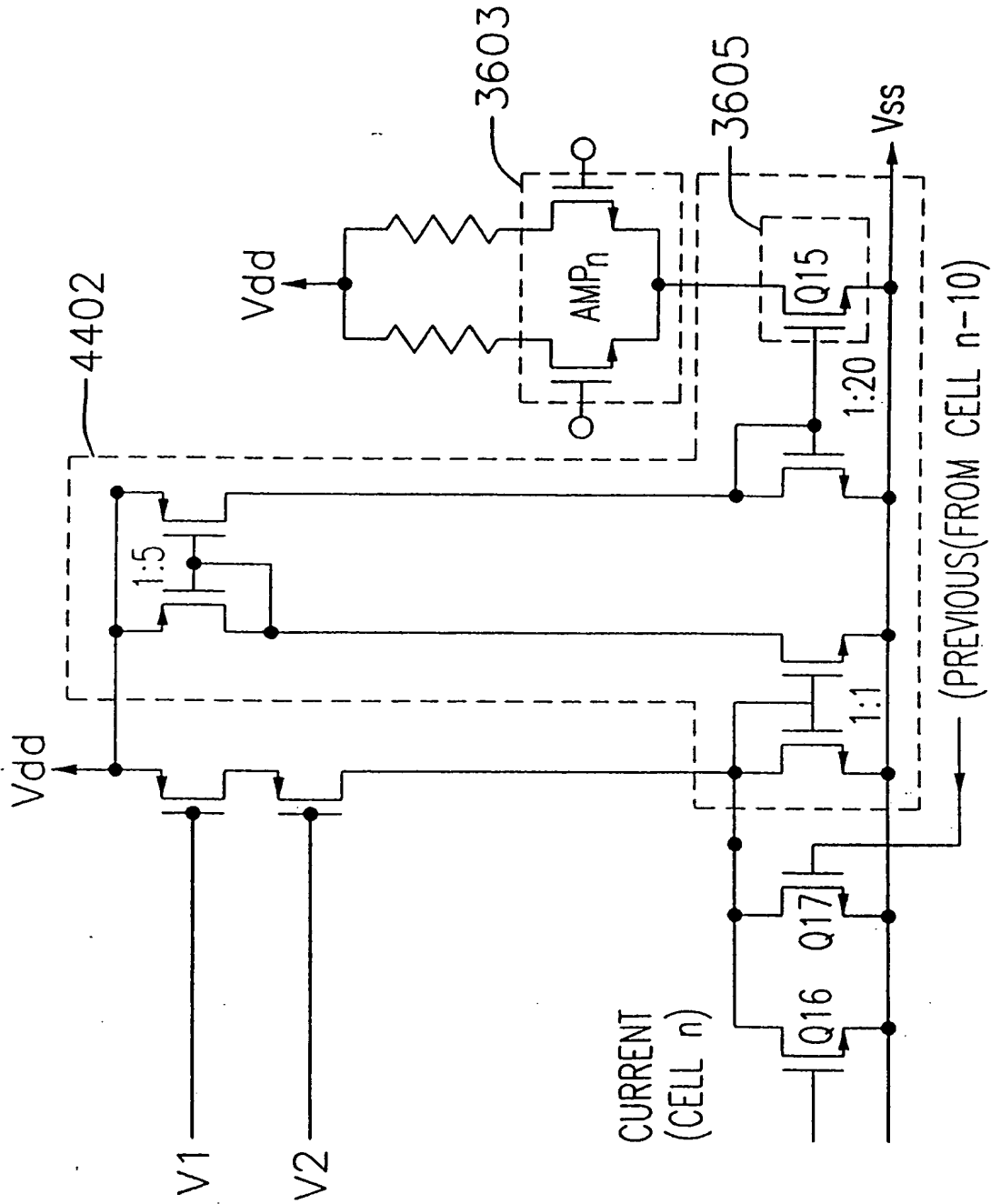


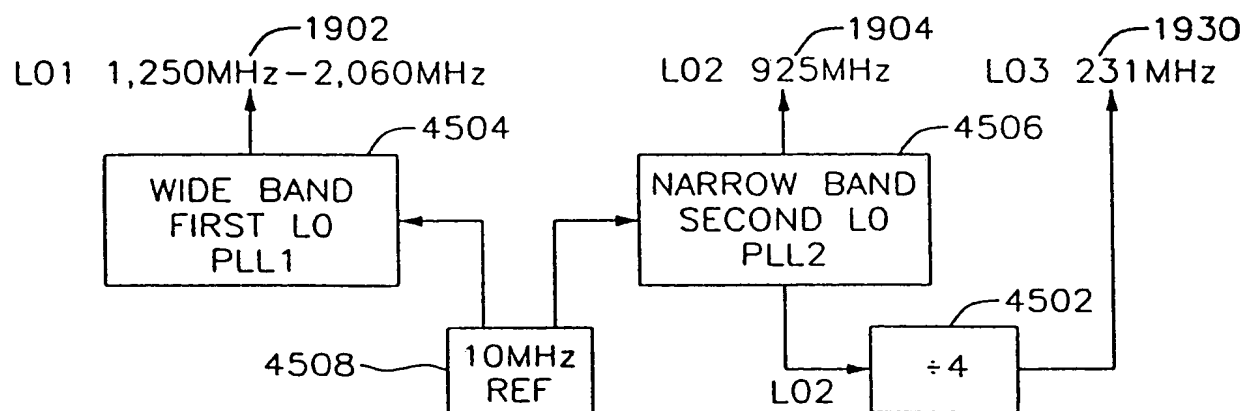
FIG. 45

FIG. 46

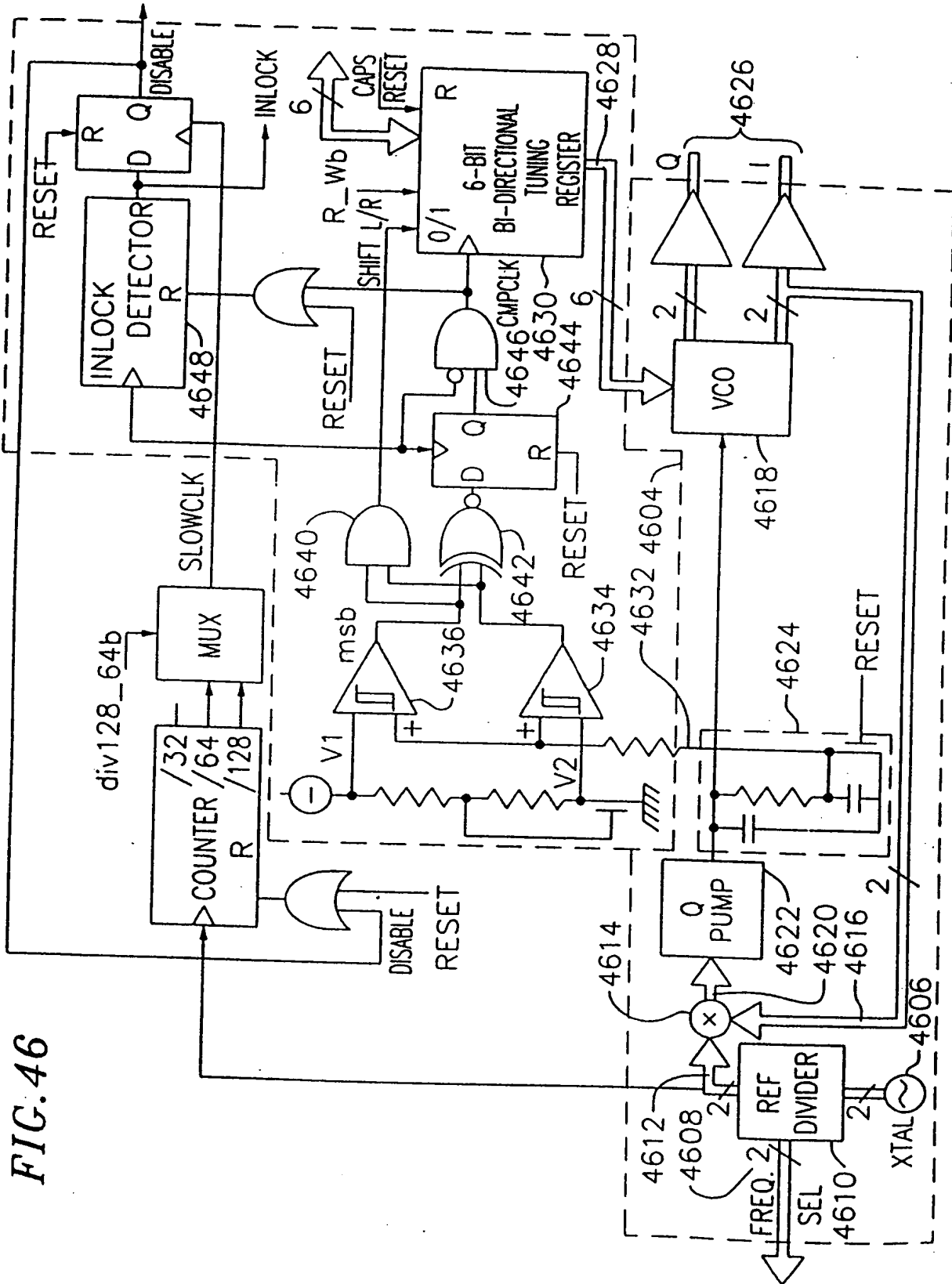
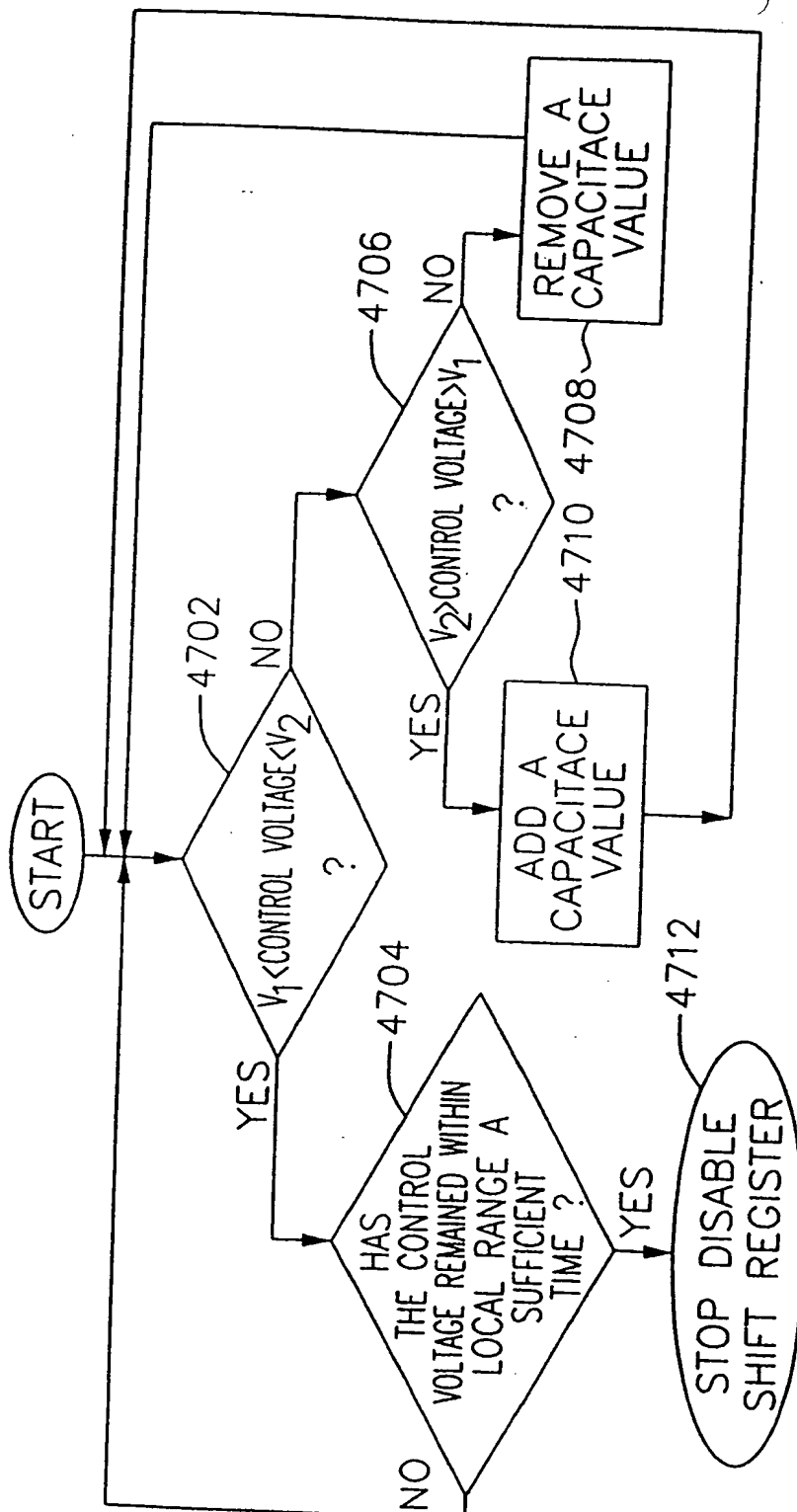


FIG. 47



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FIG. 48

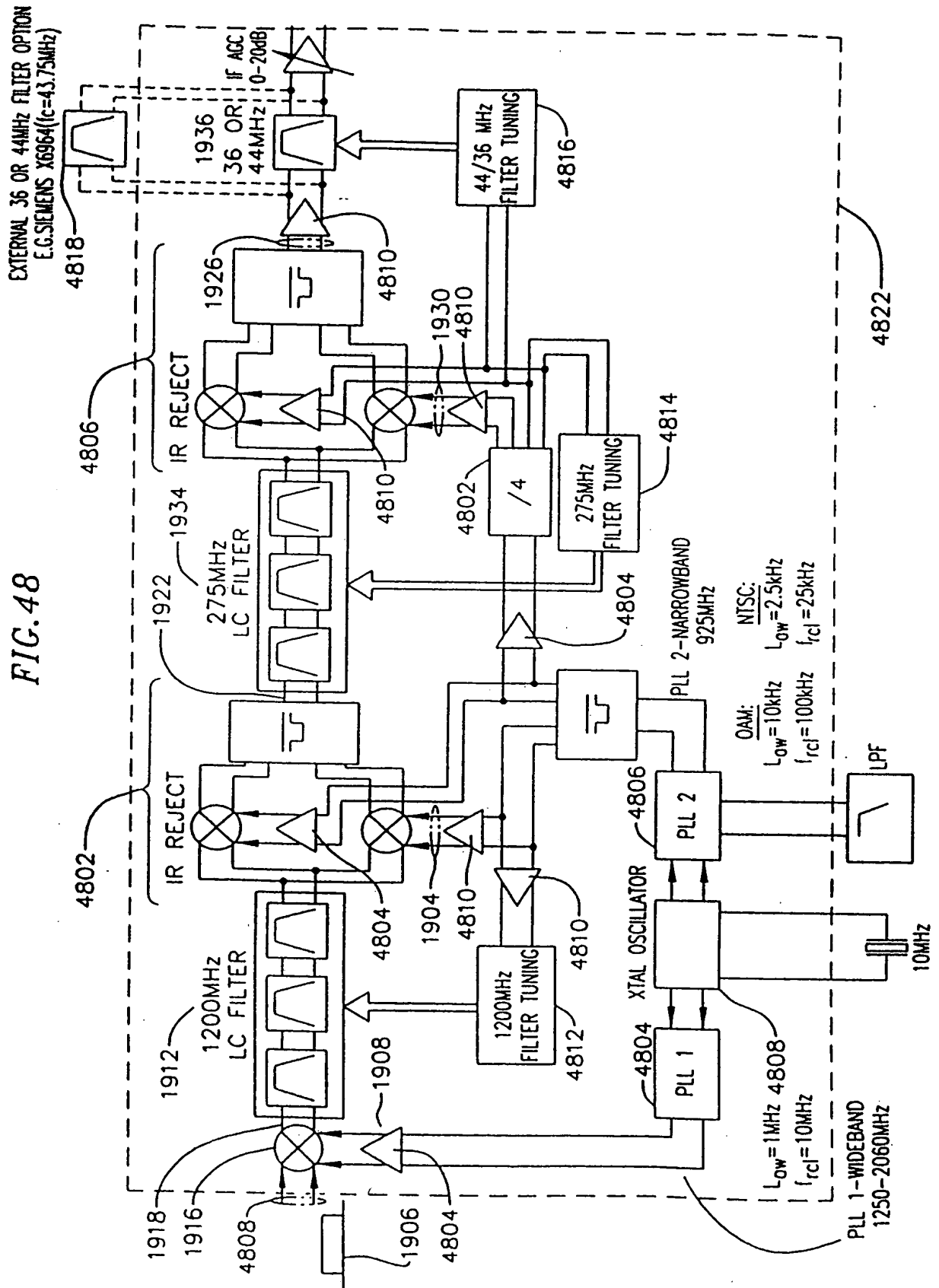


FIG. 49

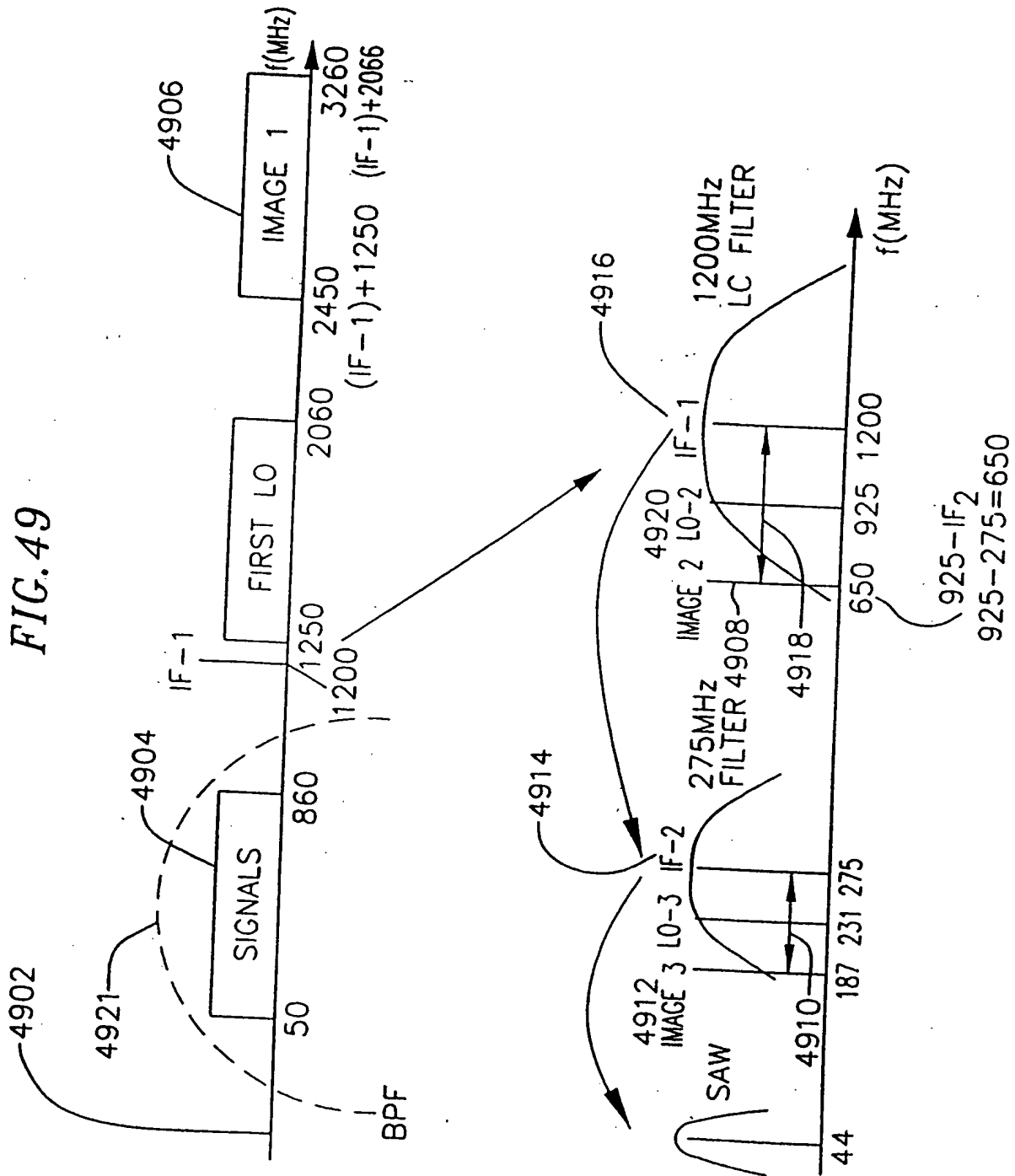
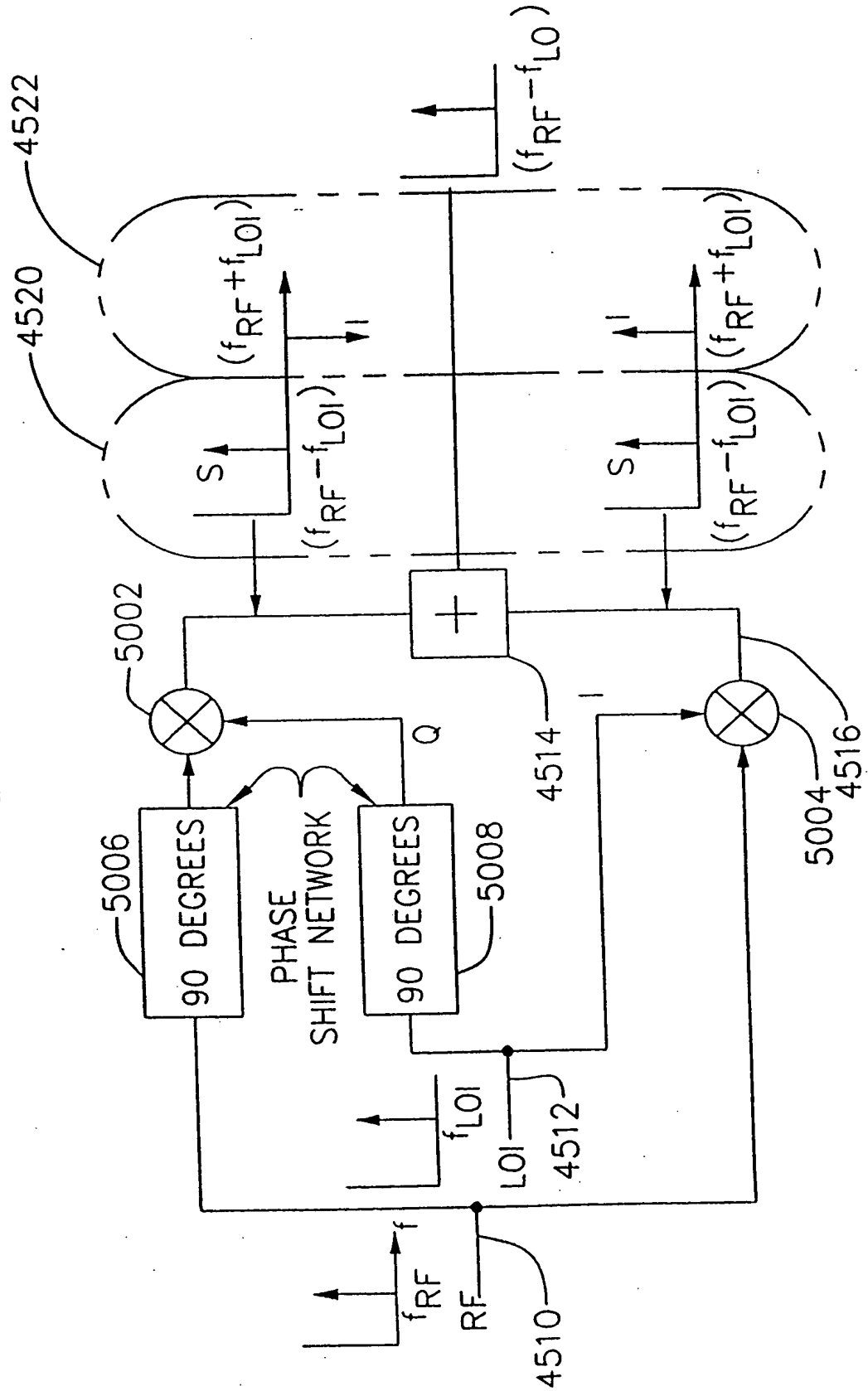
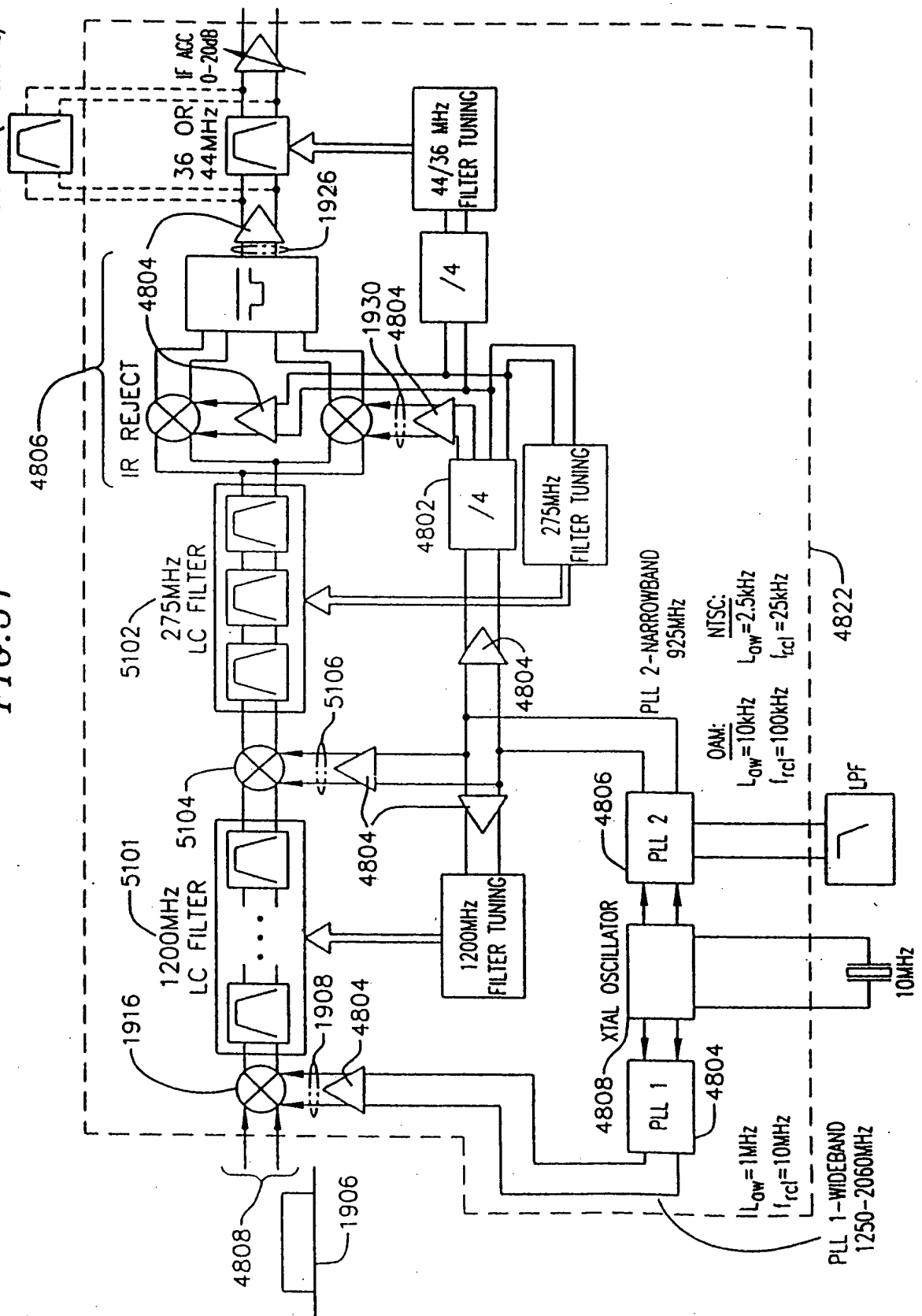


FIG. 50



EXTERNAL 36 OR 44MHz FILTER OPTION
E.G. SIEMENS X6964(f=43.75MHz)



EXTERNAL 36 OR 44MHz FILTER OPTION
E.G. SIEMENS X6964($f_c=43.75\text{MHz}$)

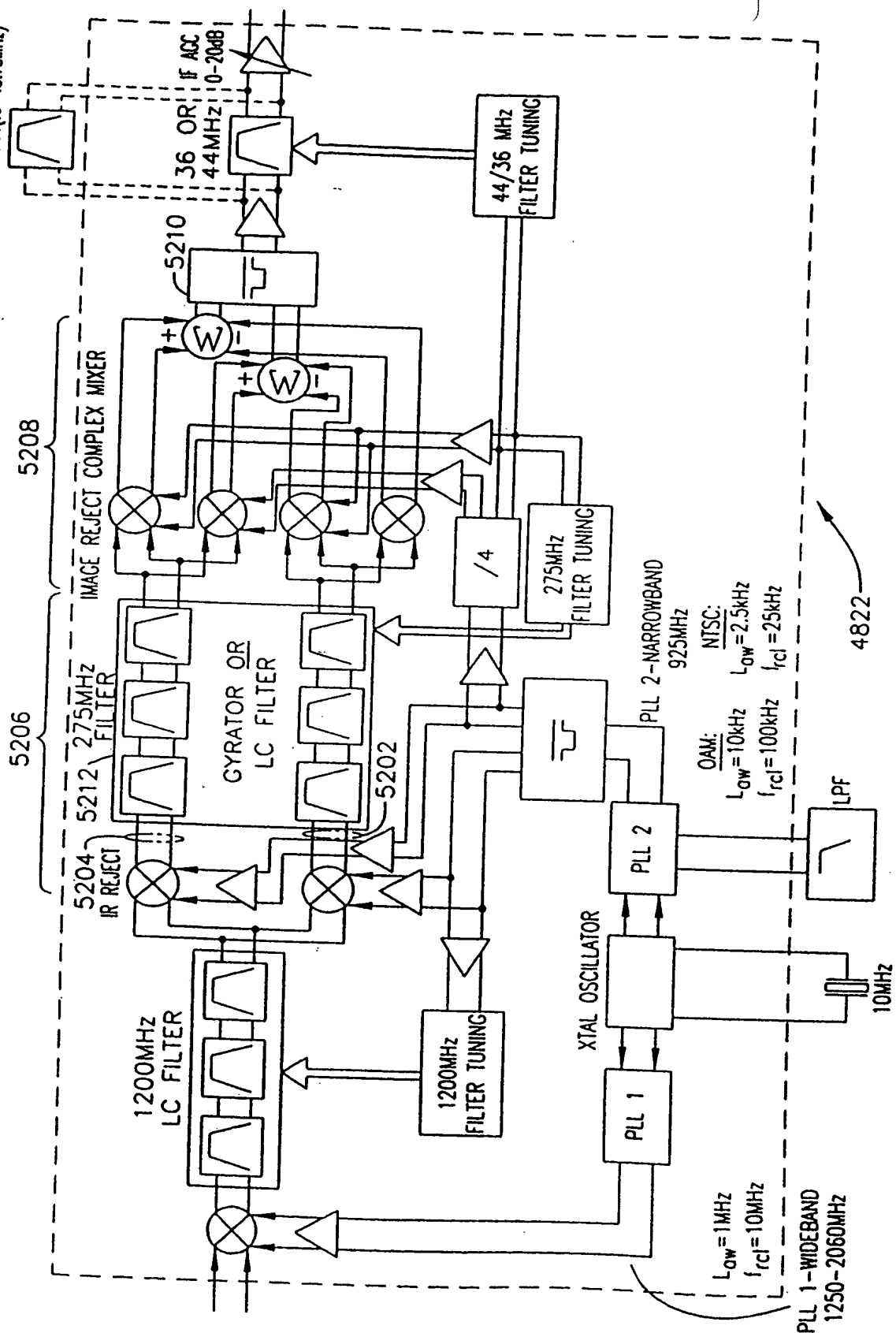
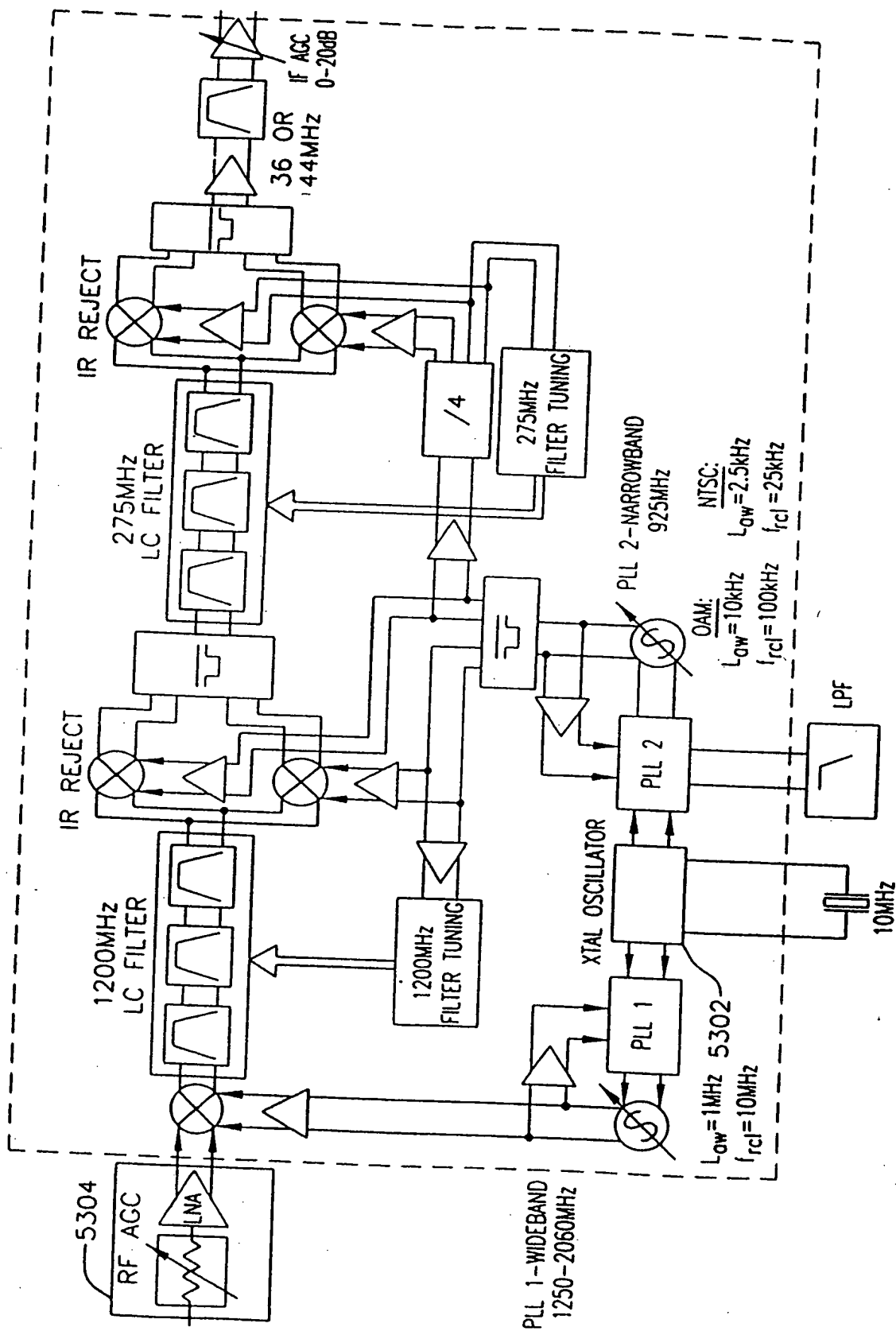
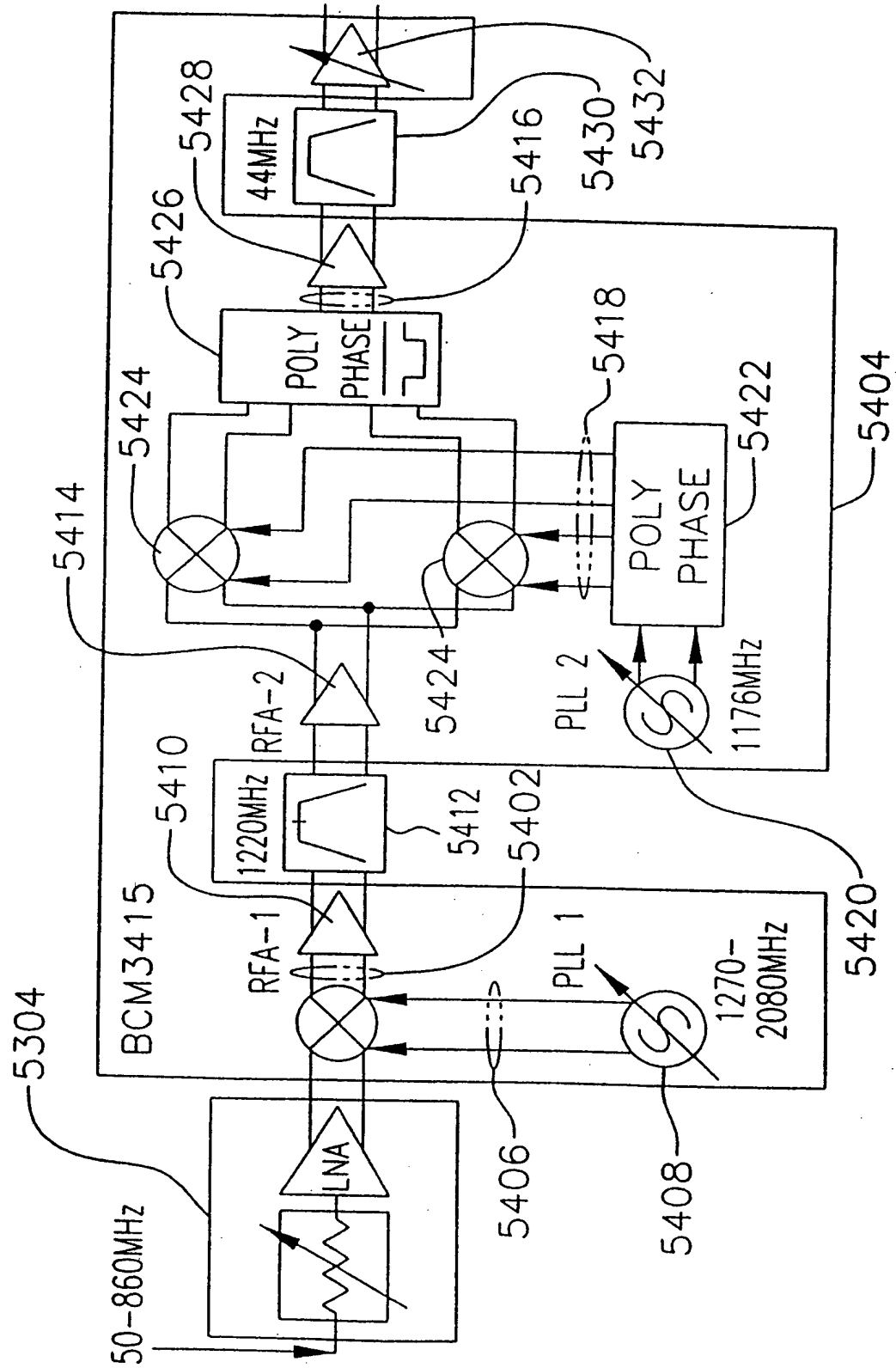


FIG. 53



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FIG. 54



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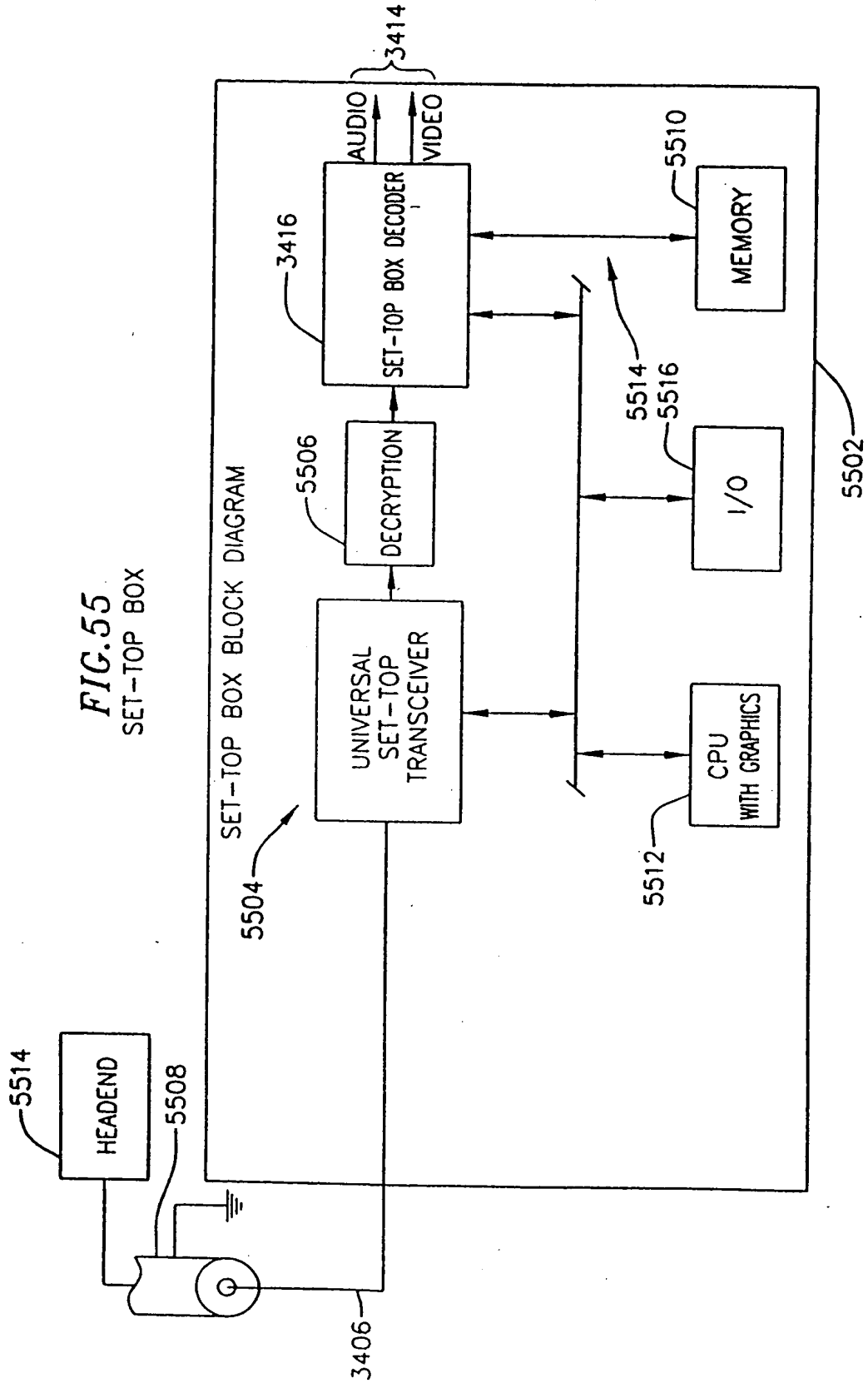
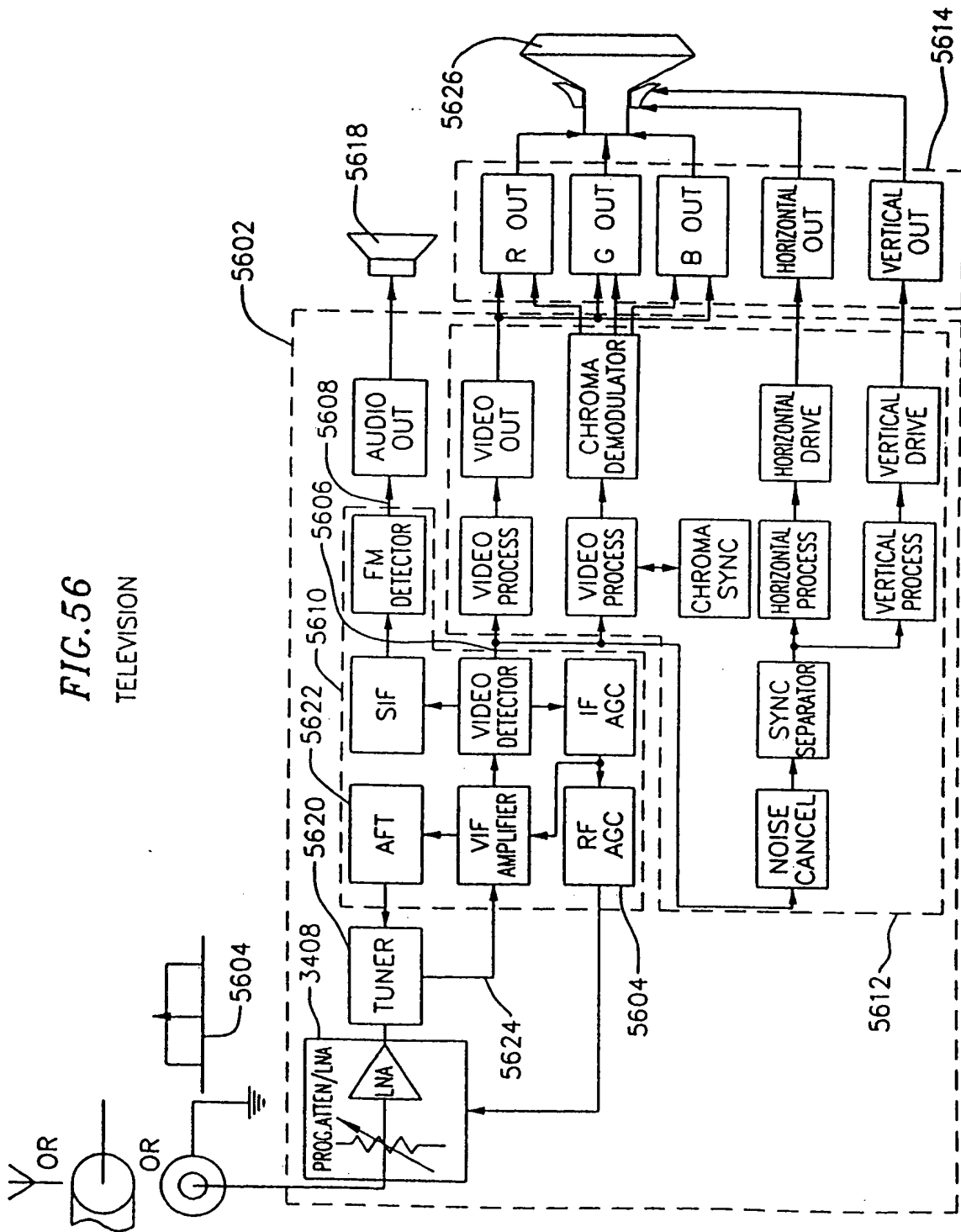


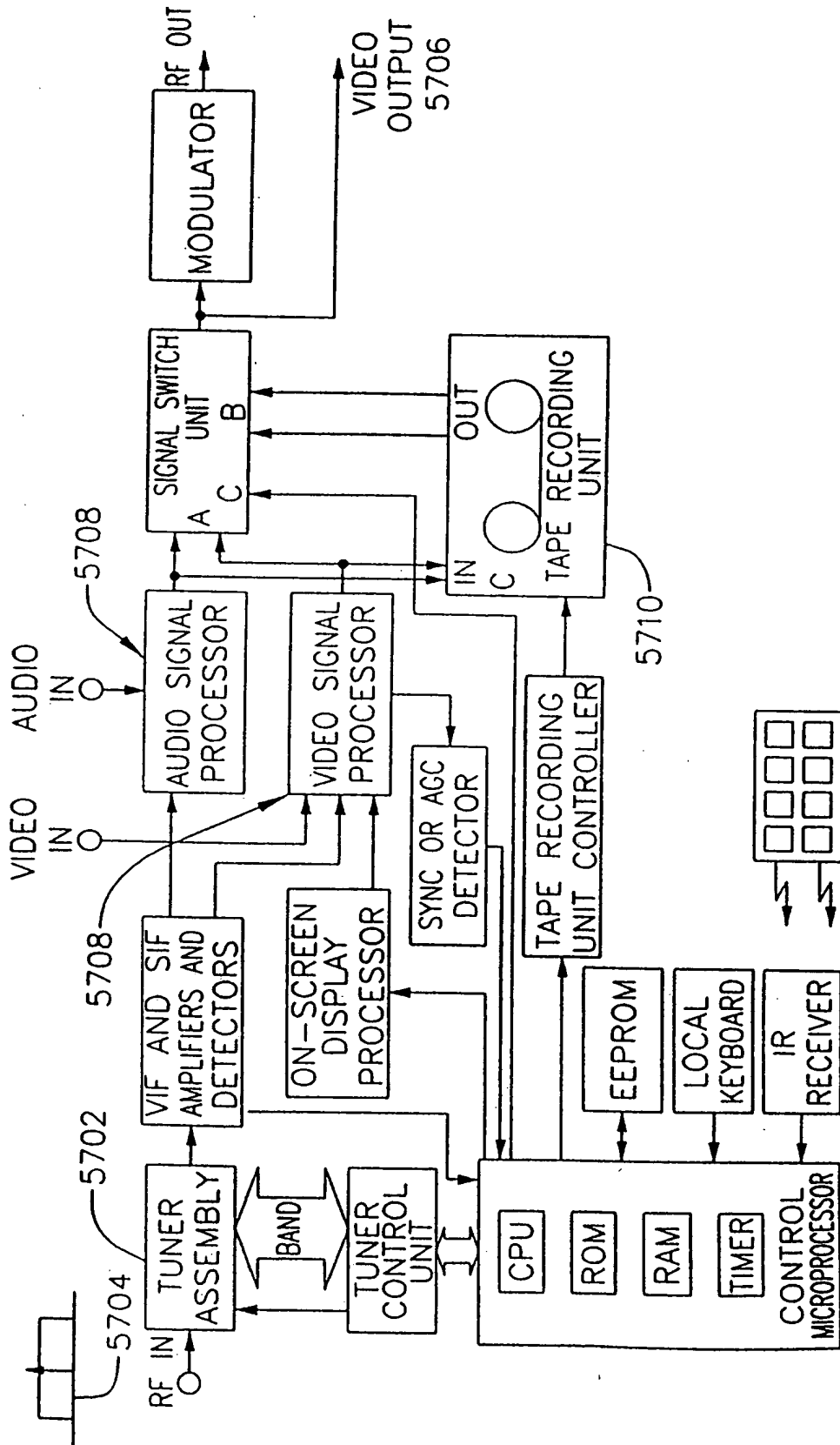
FIG. 56
TELEVISION

The diagram illustrates a television receiver system. It starts with an antenna input (V OR) and a cable input (OR) connected to a switch (5604). The signal path includes a PROCATEN/LNA block, a TUNER (5620), an AFT (5622), an SIF (5610), an FM DETECTOR (5606), an AUDIO OUT (5618), a VIDEO DETECTOR (5624), a VIDEO PROCESS (5612), a VIDEO OUT (5608), a VIF AMPLIFIER (5624), an RF AGC (5604), an IF AGC (5624), a CHROMA SYNC (5612), a CHROMA DEMODULATOR (5612), a CHROMA OUT (5618), a B OUT (5618), a G OUT (5618), an R OUT (5618), a HORIZONTAL DRIVE (5614), a HORIZONTAL OUT (5614), a VERTICAL DRIVE (5614), and a VERTICAL OUT (5614). The diagram shows the flow of signals from input to output, with various control and processing blocks in between.



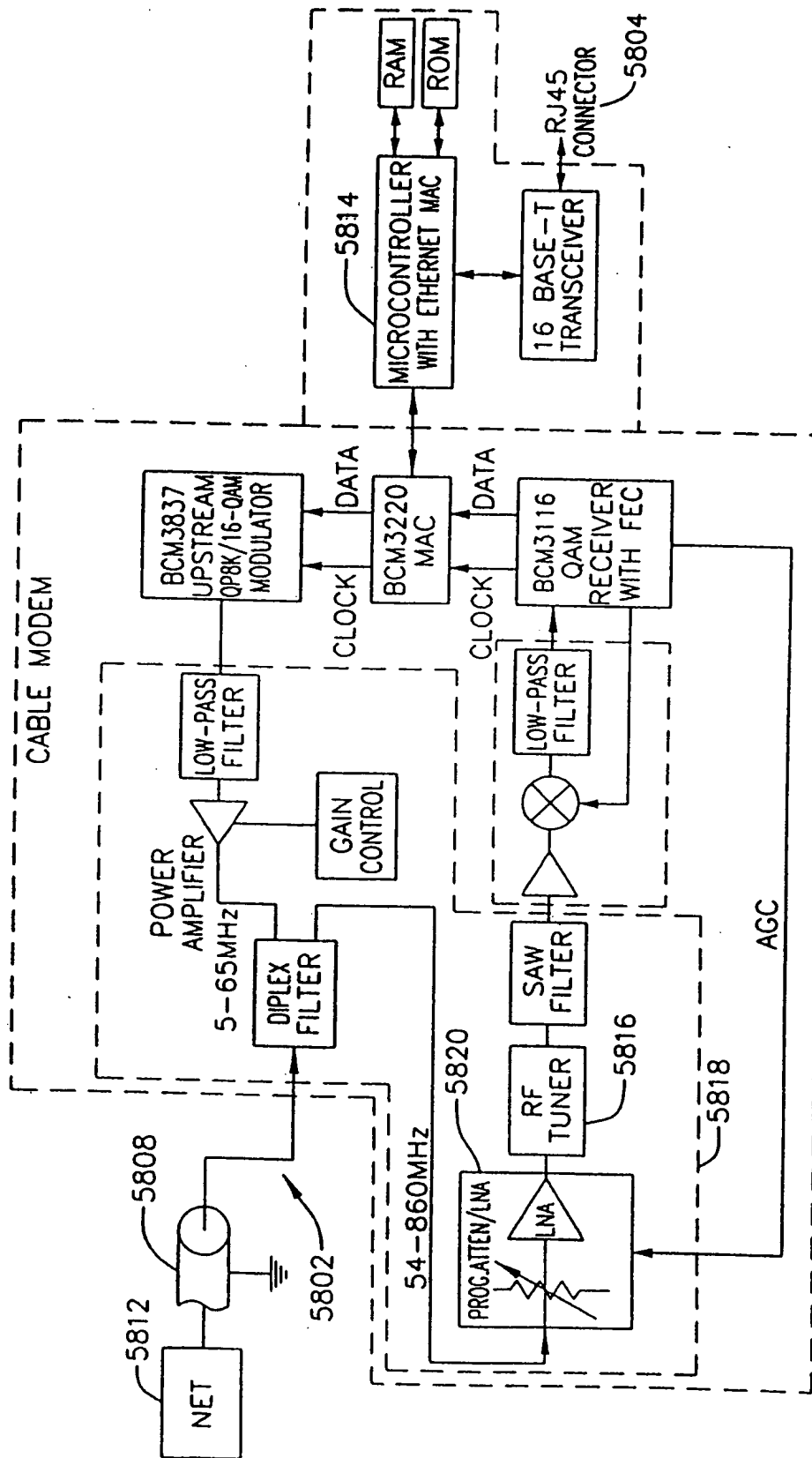
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FIG. 57
 VCR BLOCK DIAGRAM



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FIG. 58



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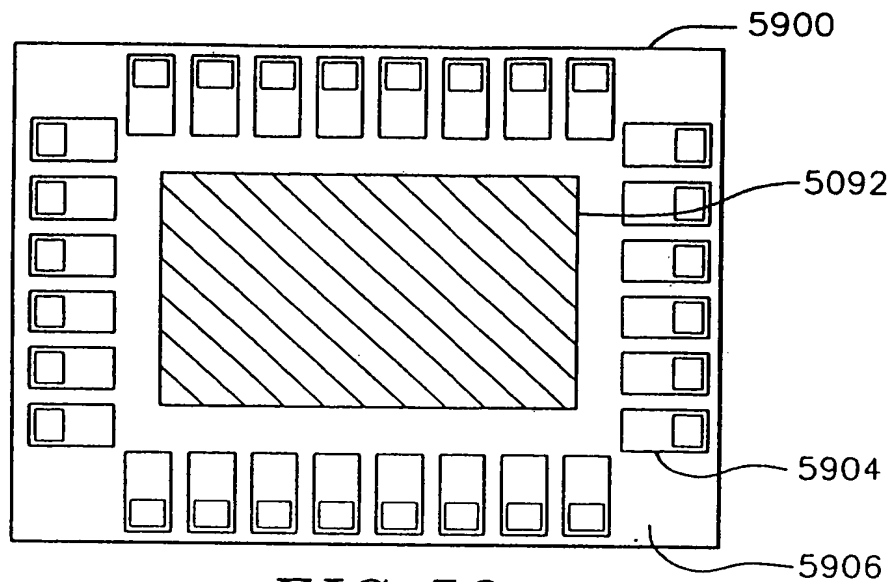


FIG. 59

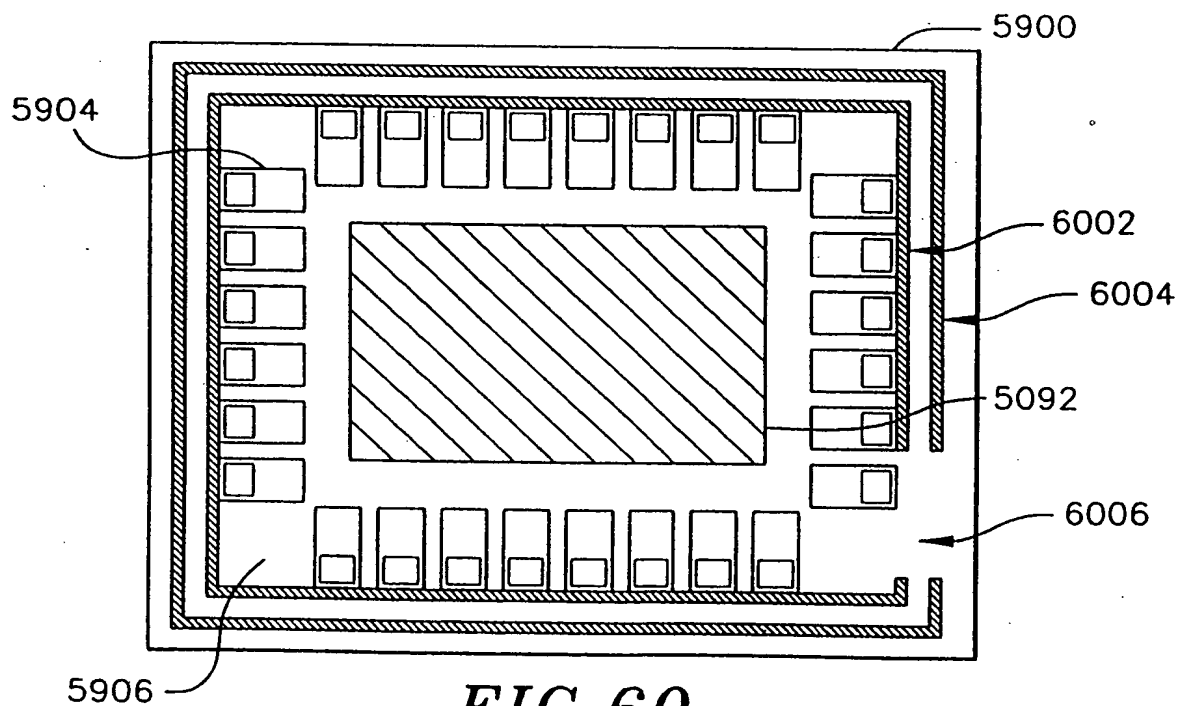


FIG. 60

FIG. 61

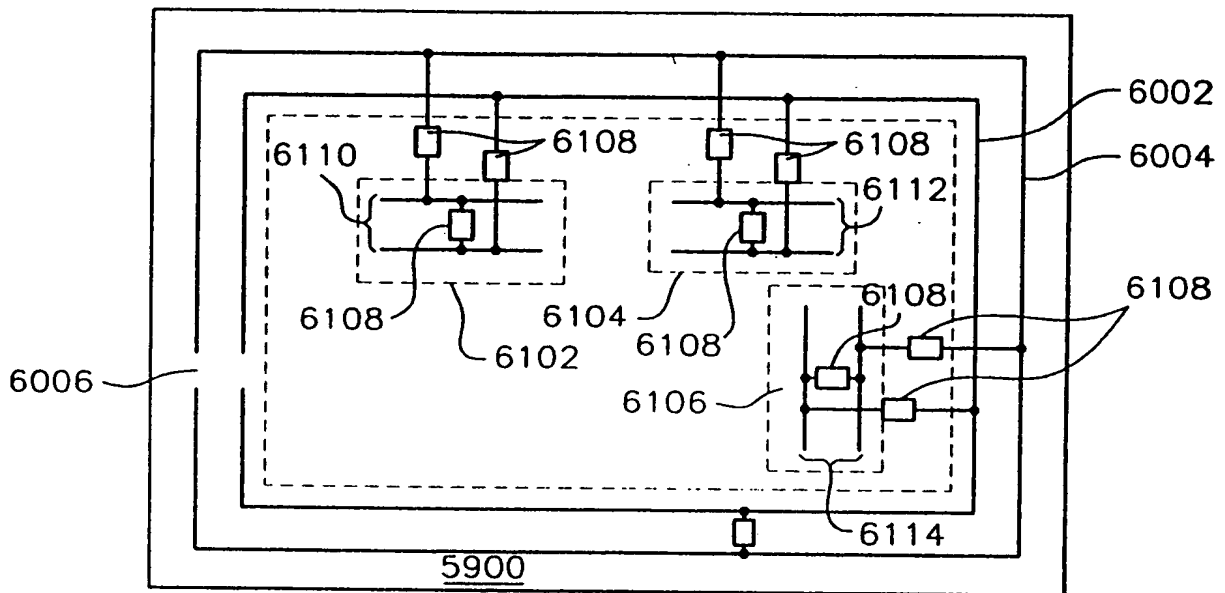


FIG. 62

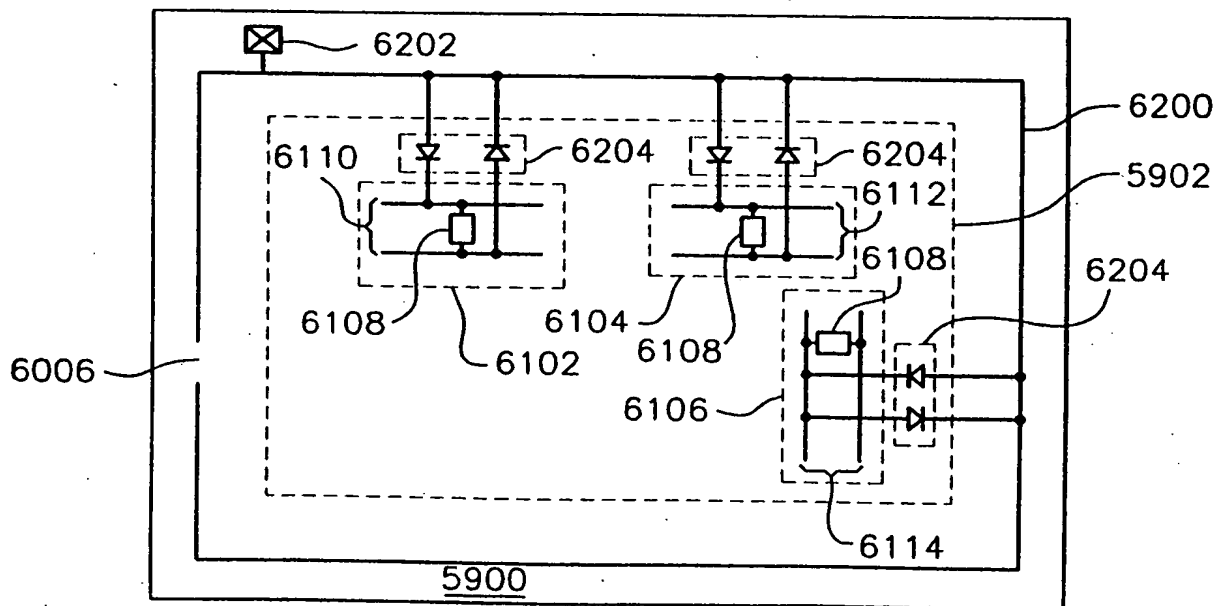
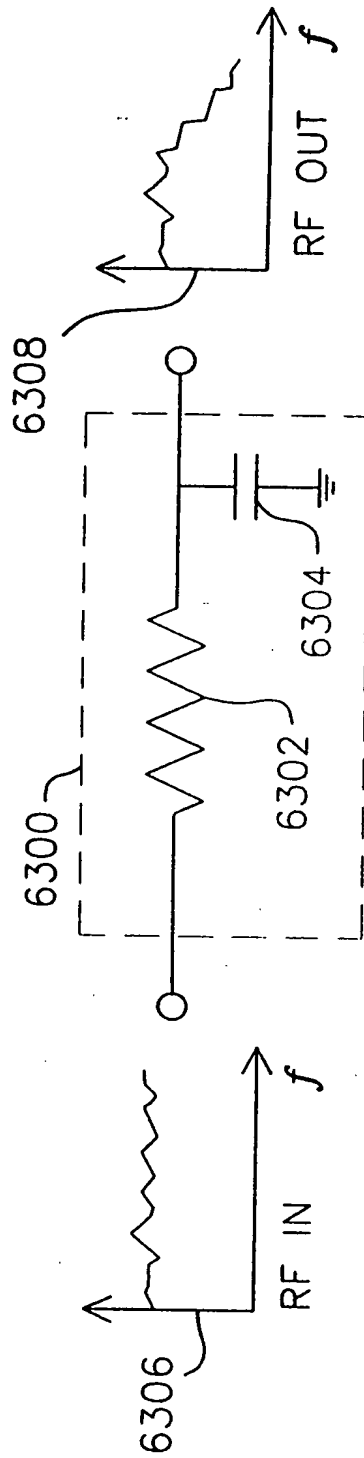


FIG. 63



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FIG. 64

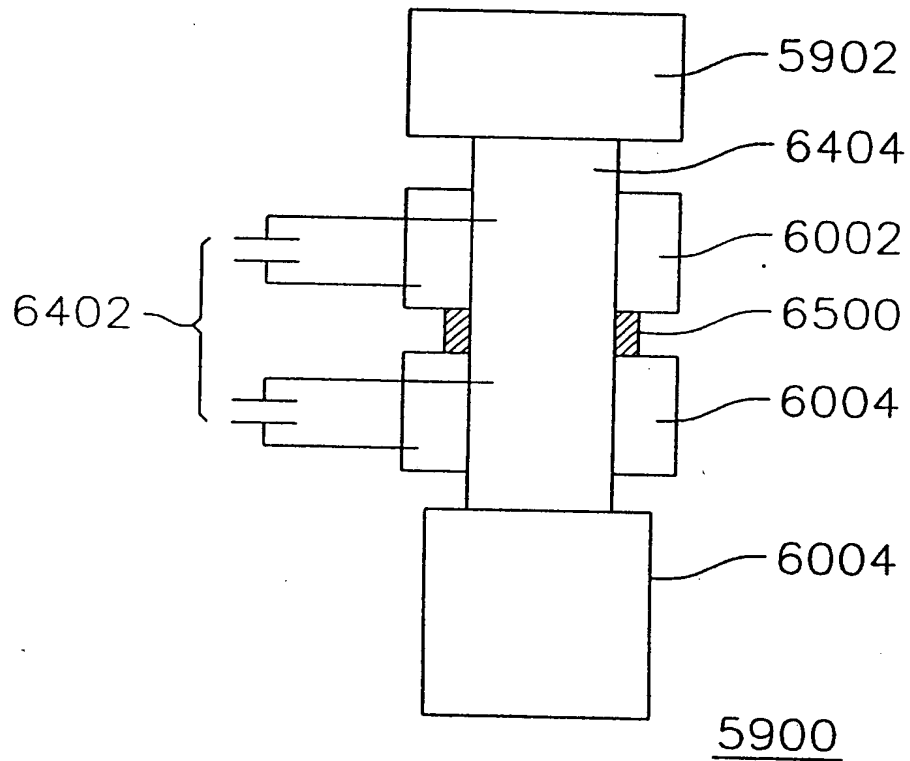


FIG. 65

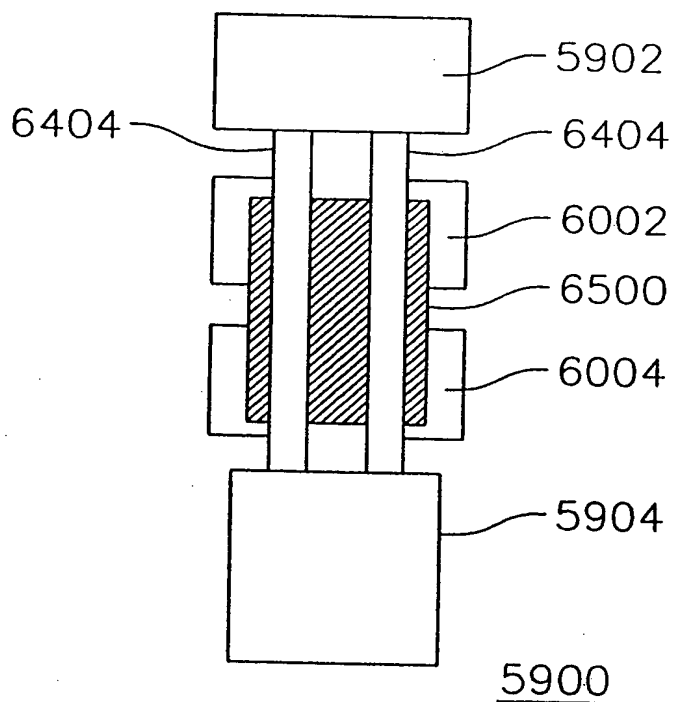


FIG. 66

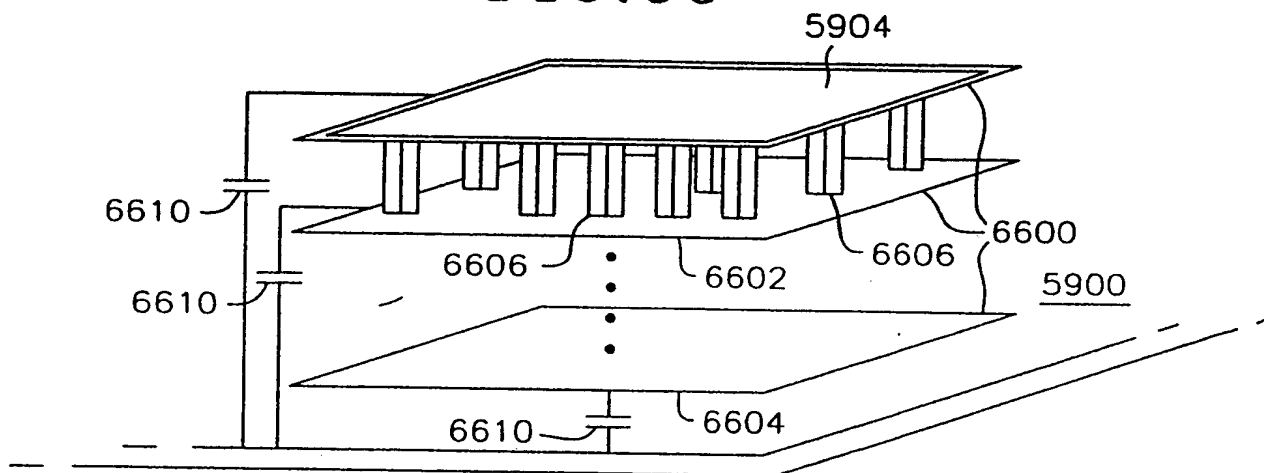
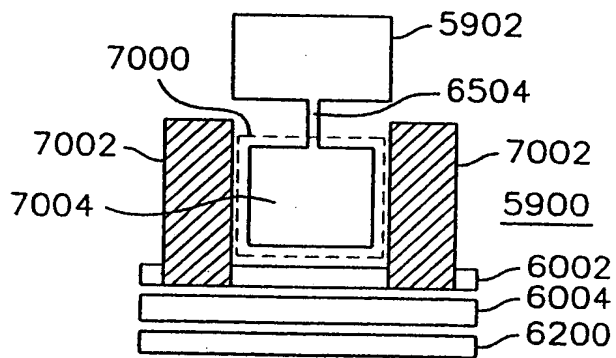
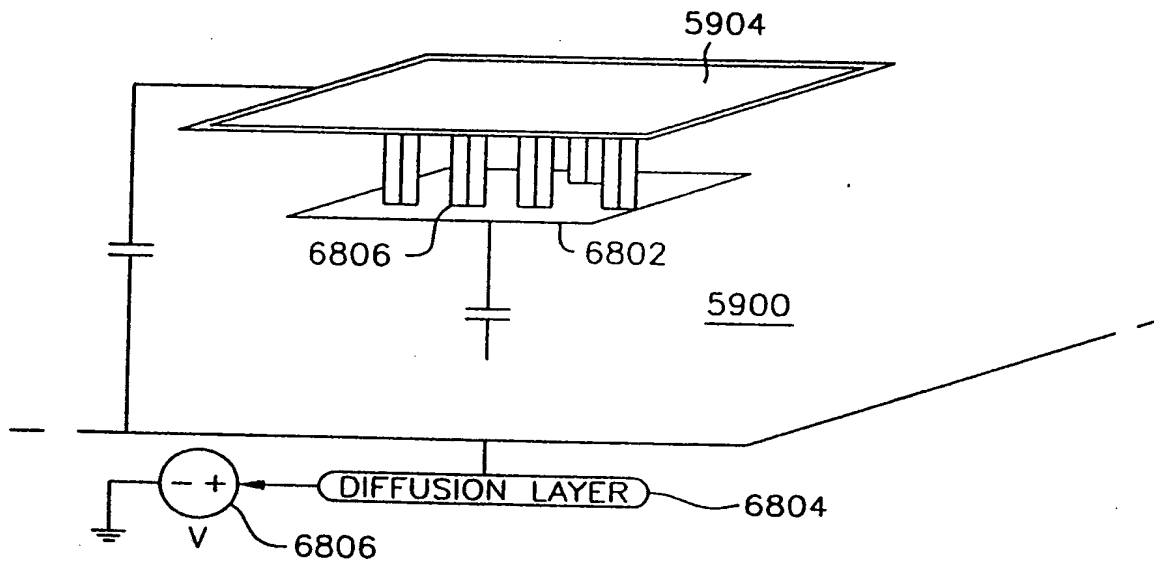


FIG. 67



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FIG. 68



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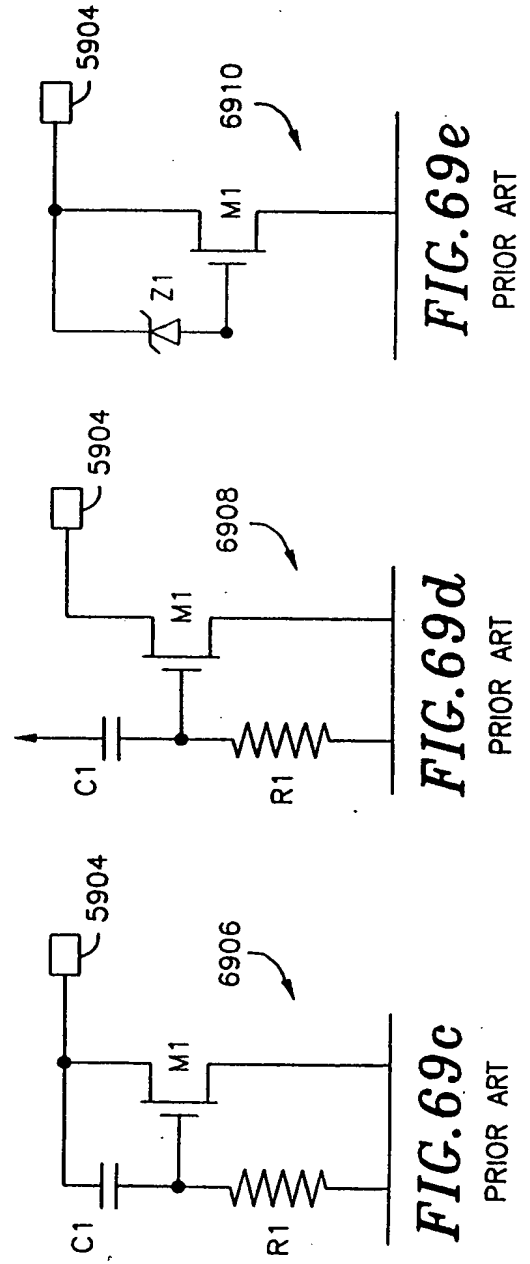
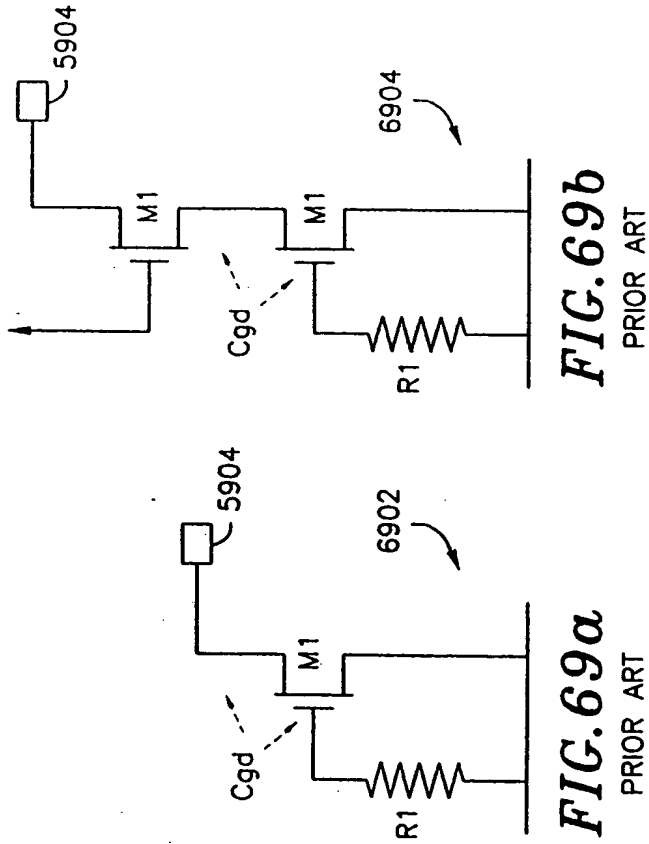
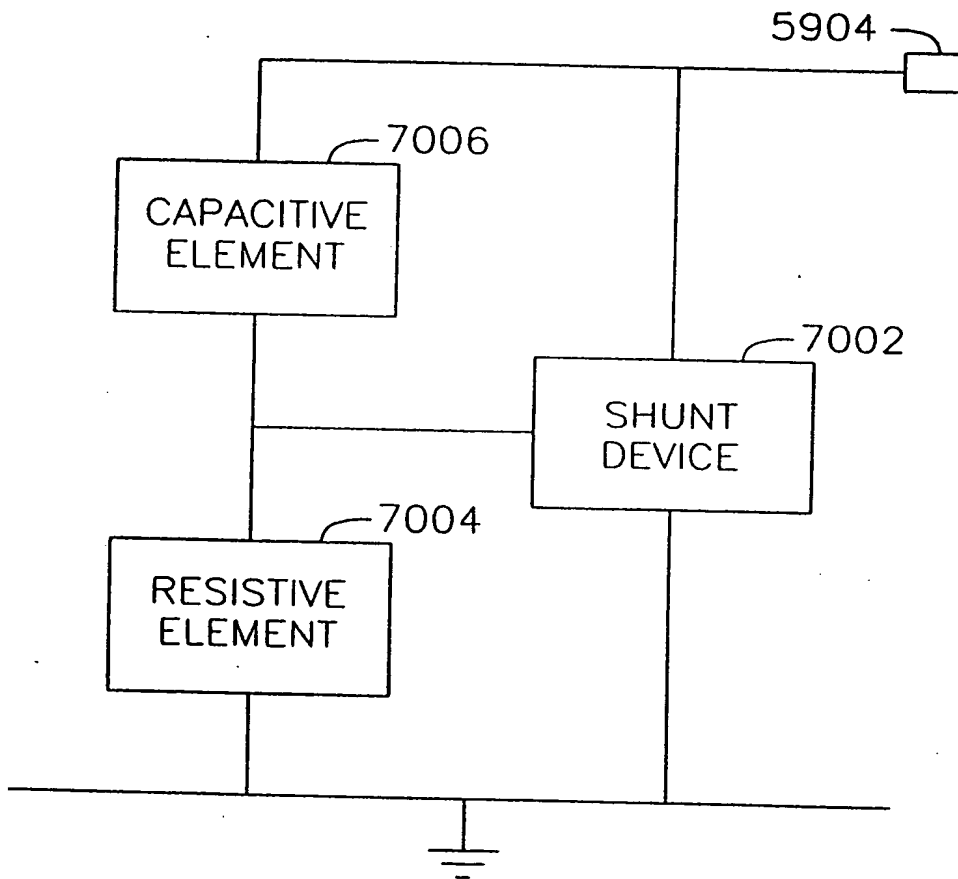
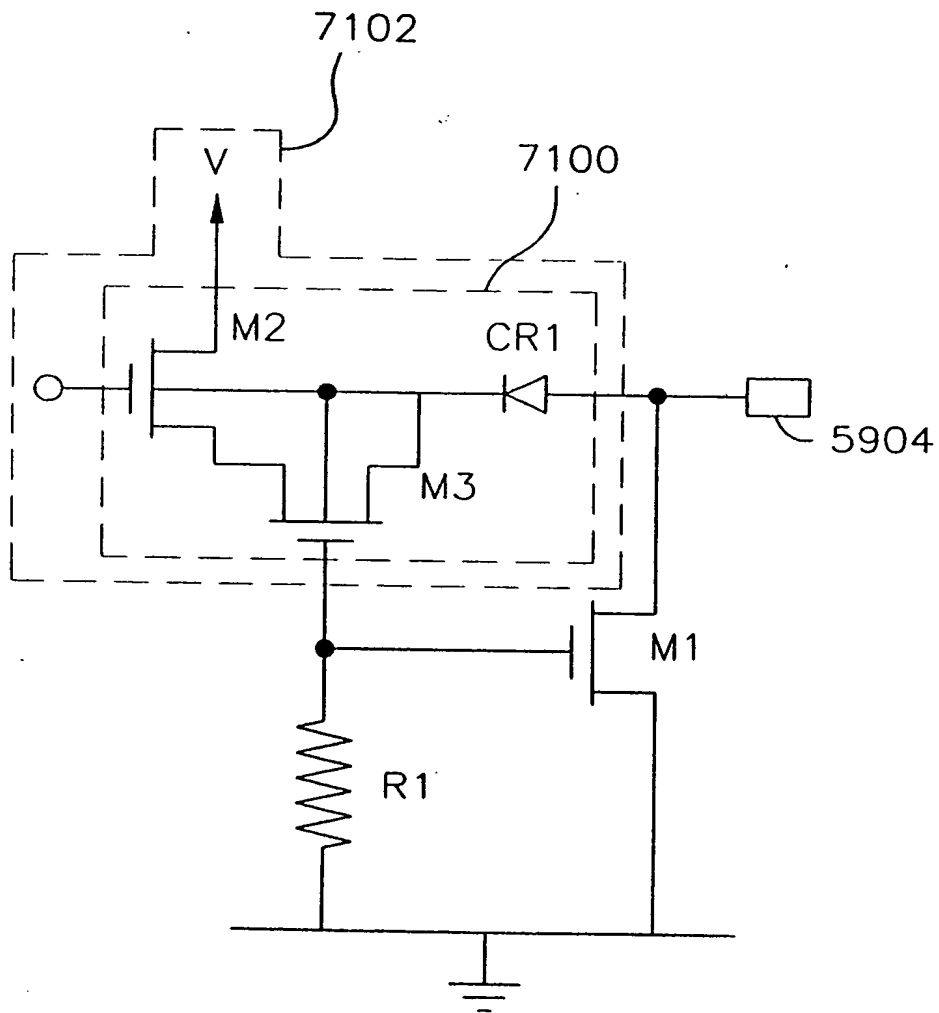
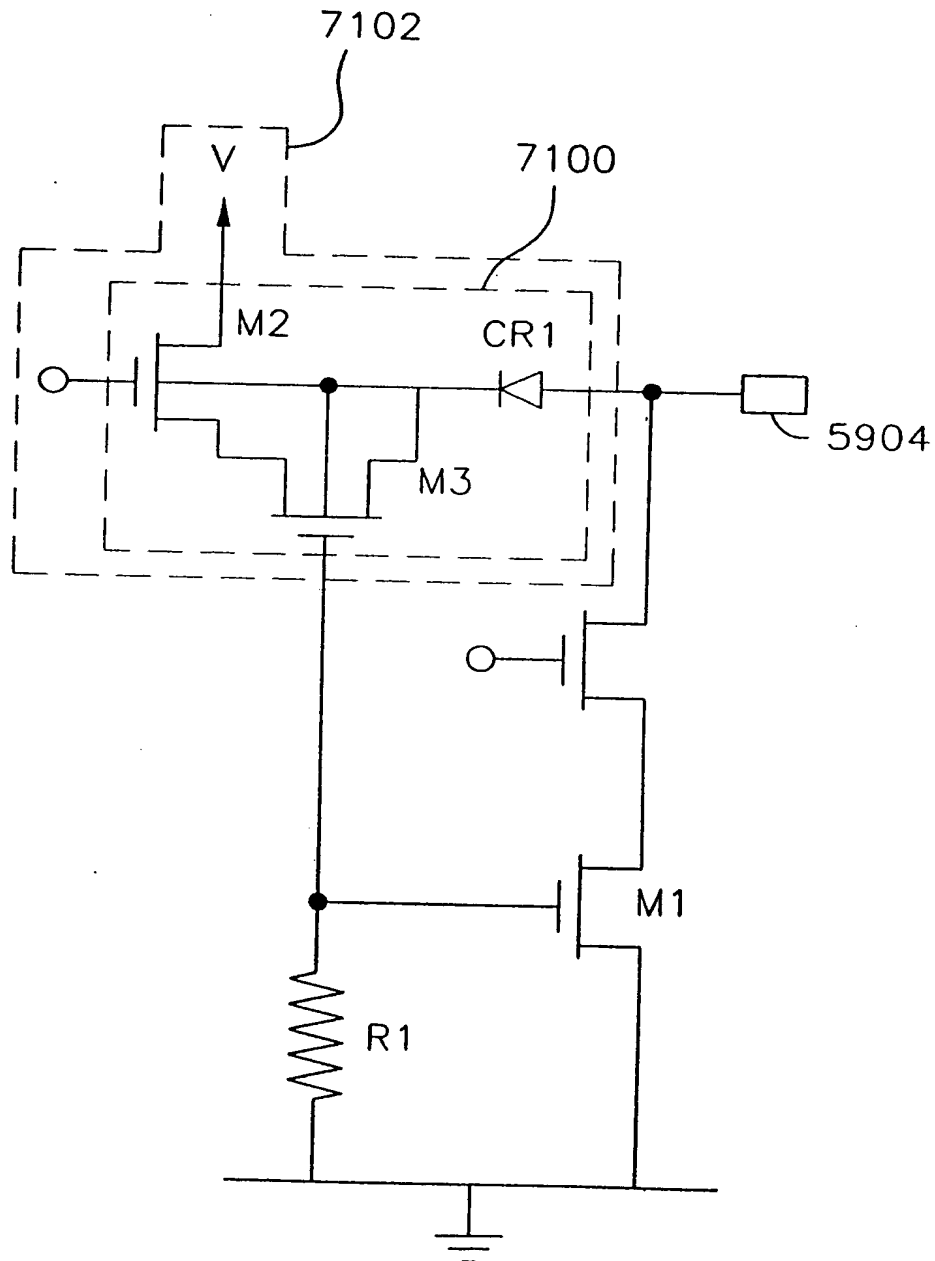


FIG. 70

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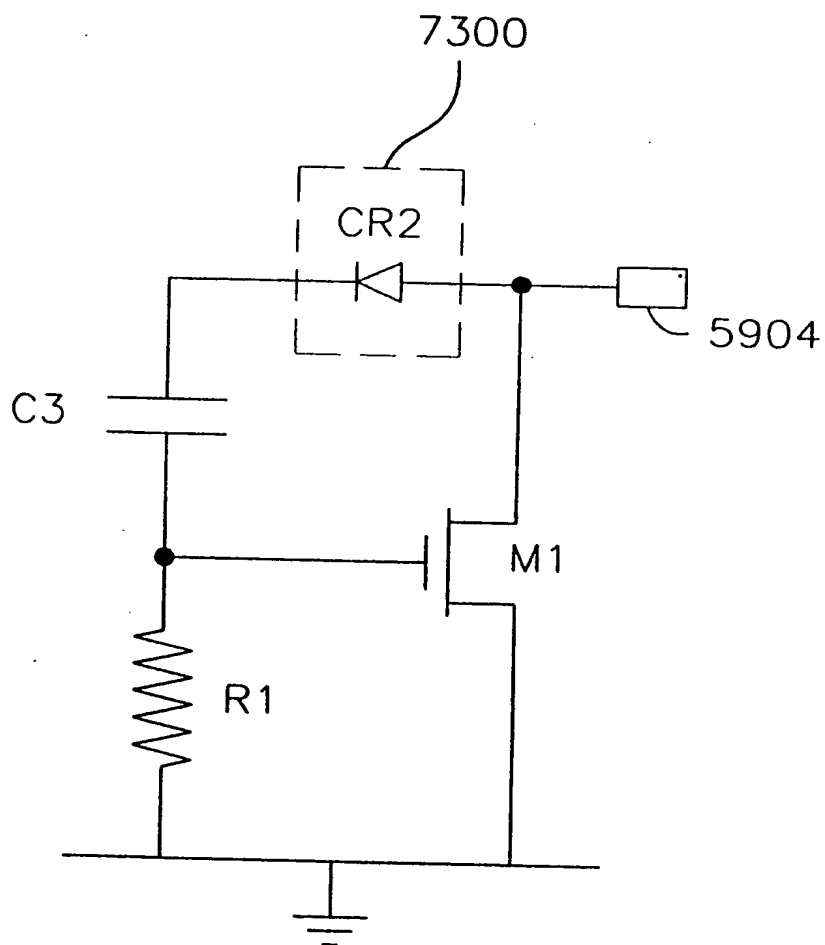
FIG. 71

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FIG. 72

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FIG. 73



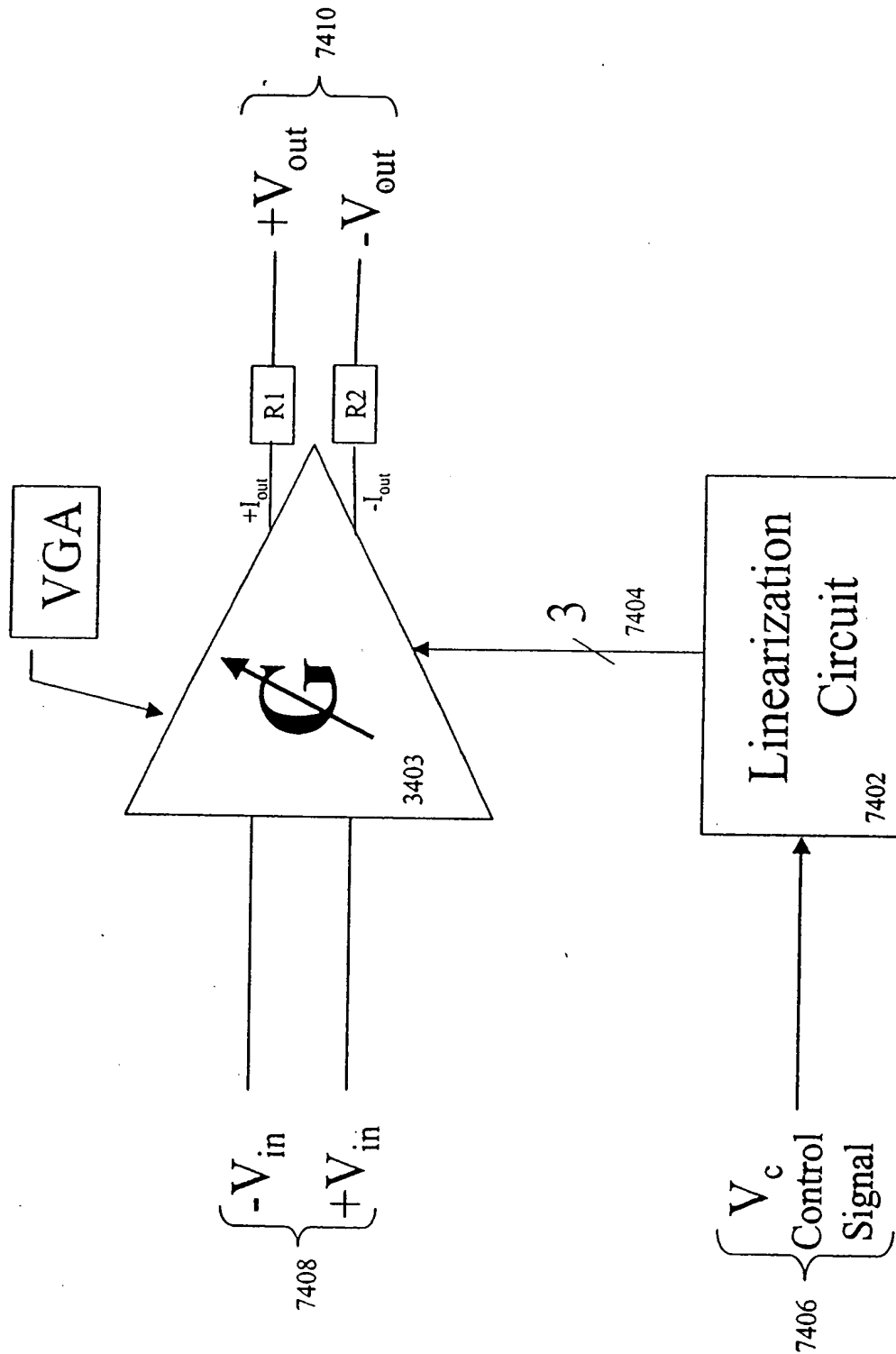


FIG. 74

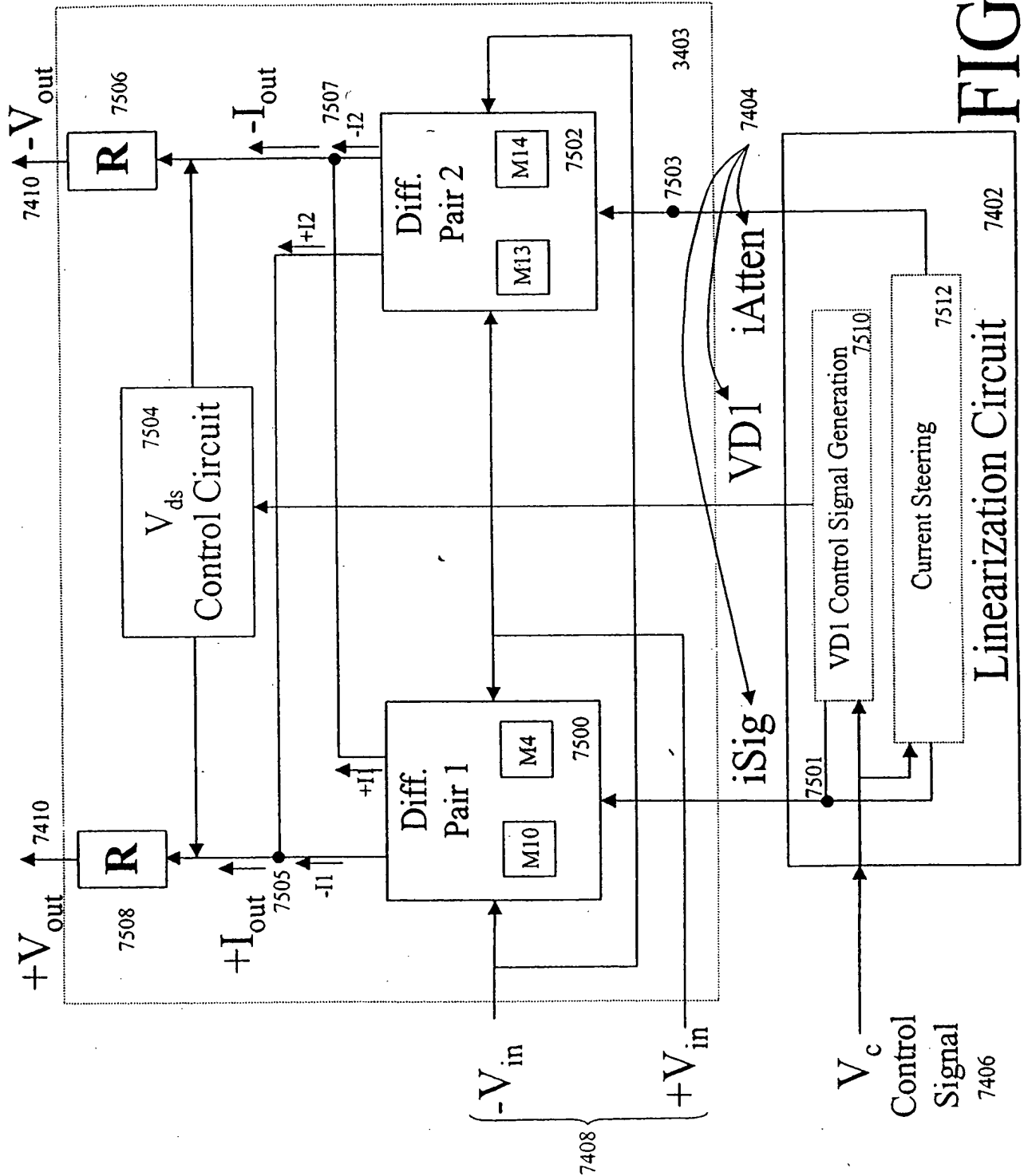


FIG. 75

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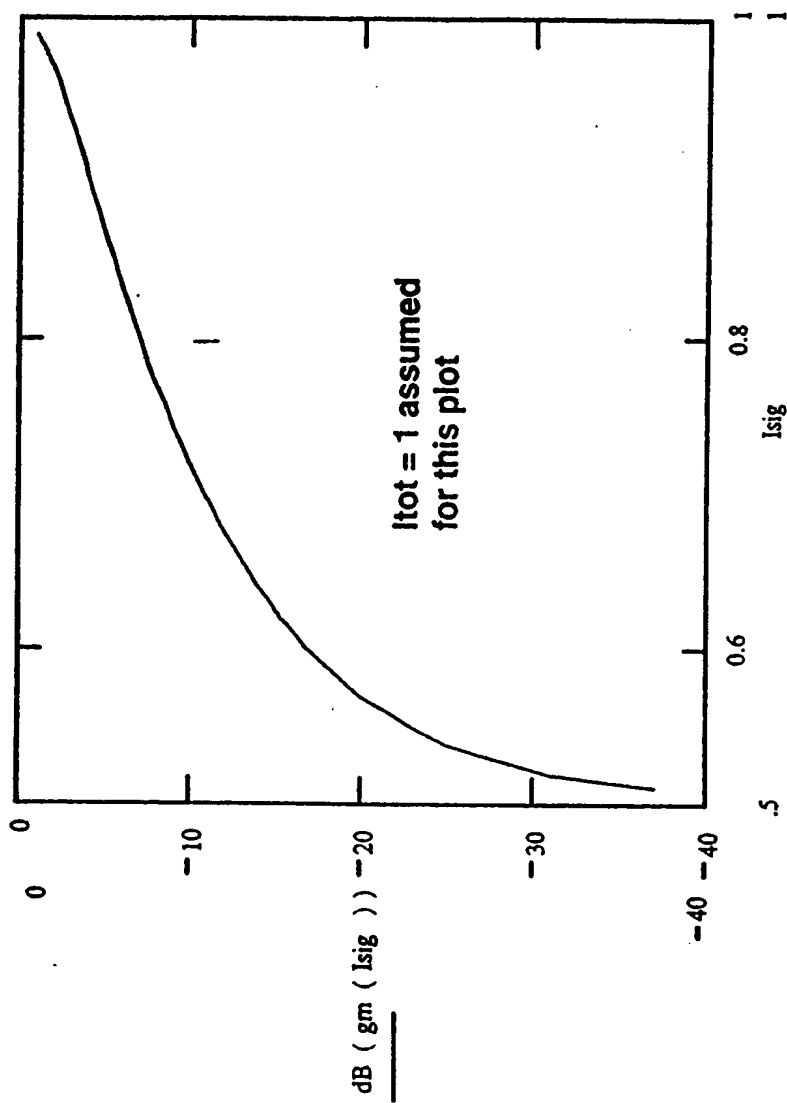


FIG 76

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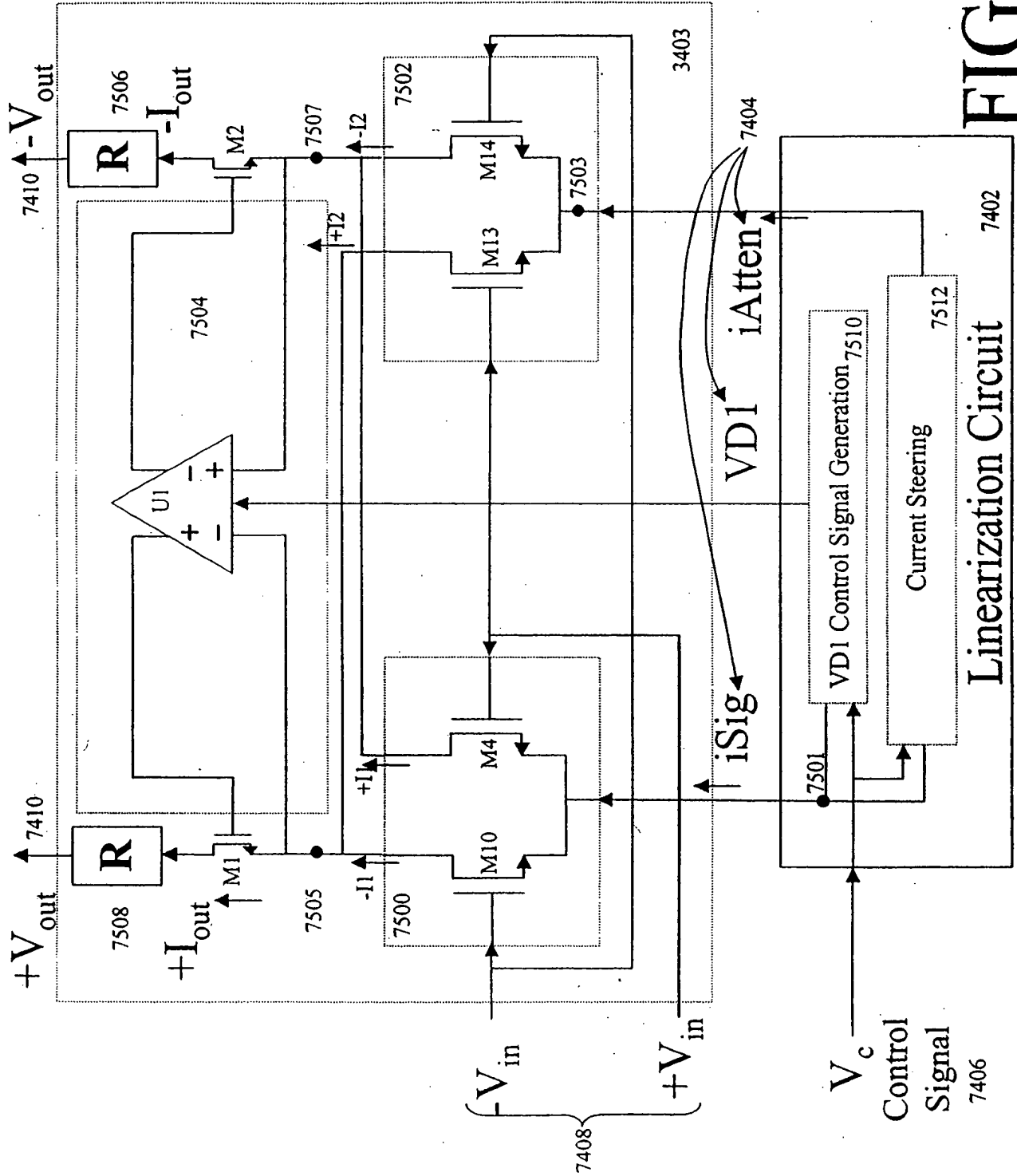


FIG. 77

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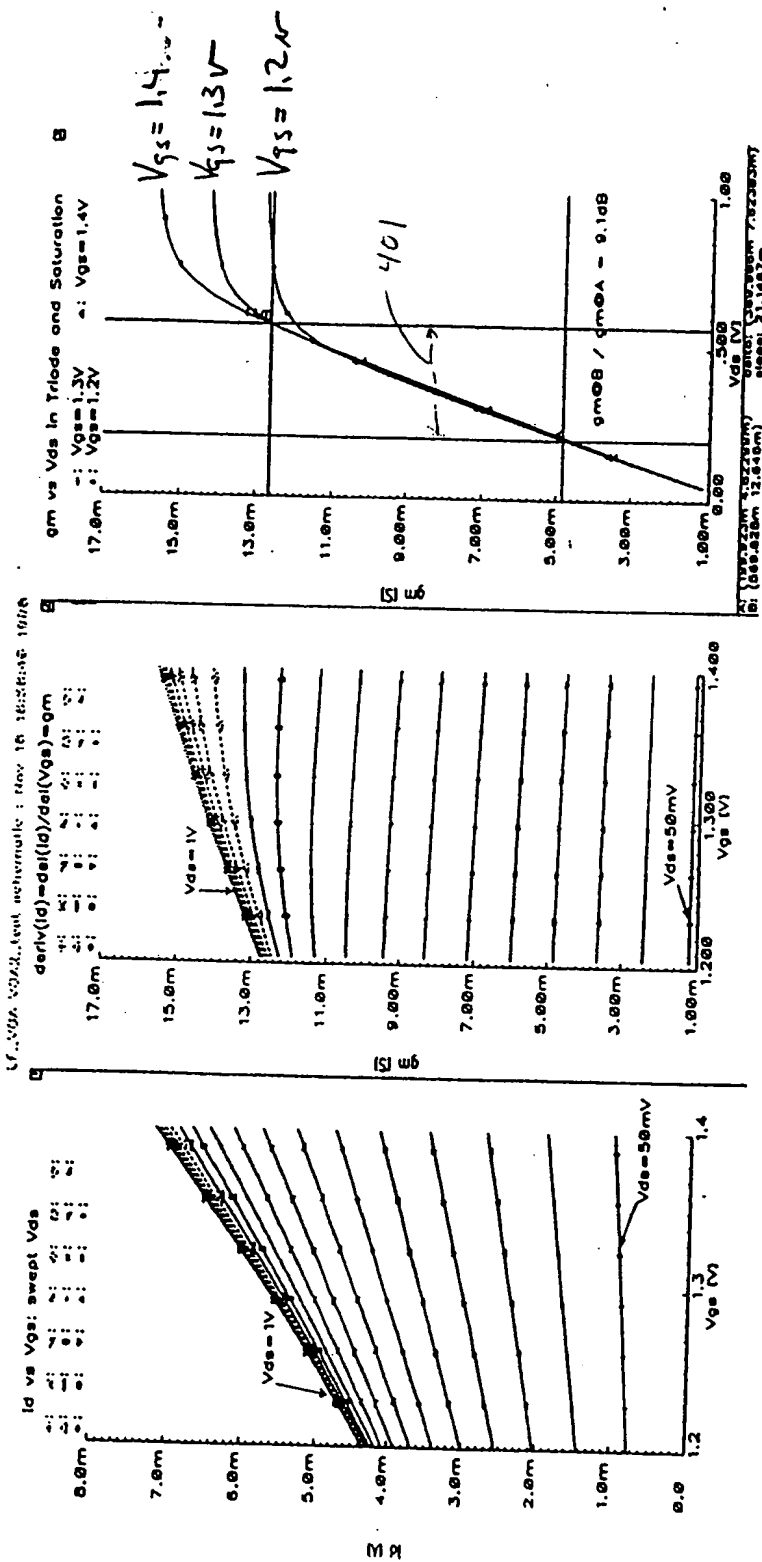


FIG 78a

FIG 78b

FIG 78c

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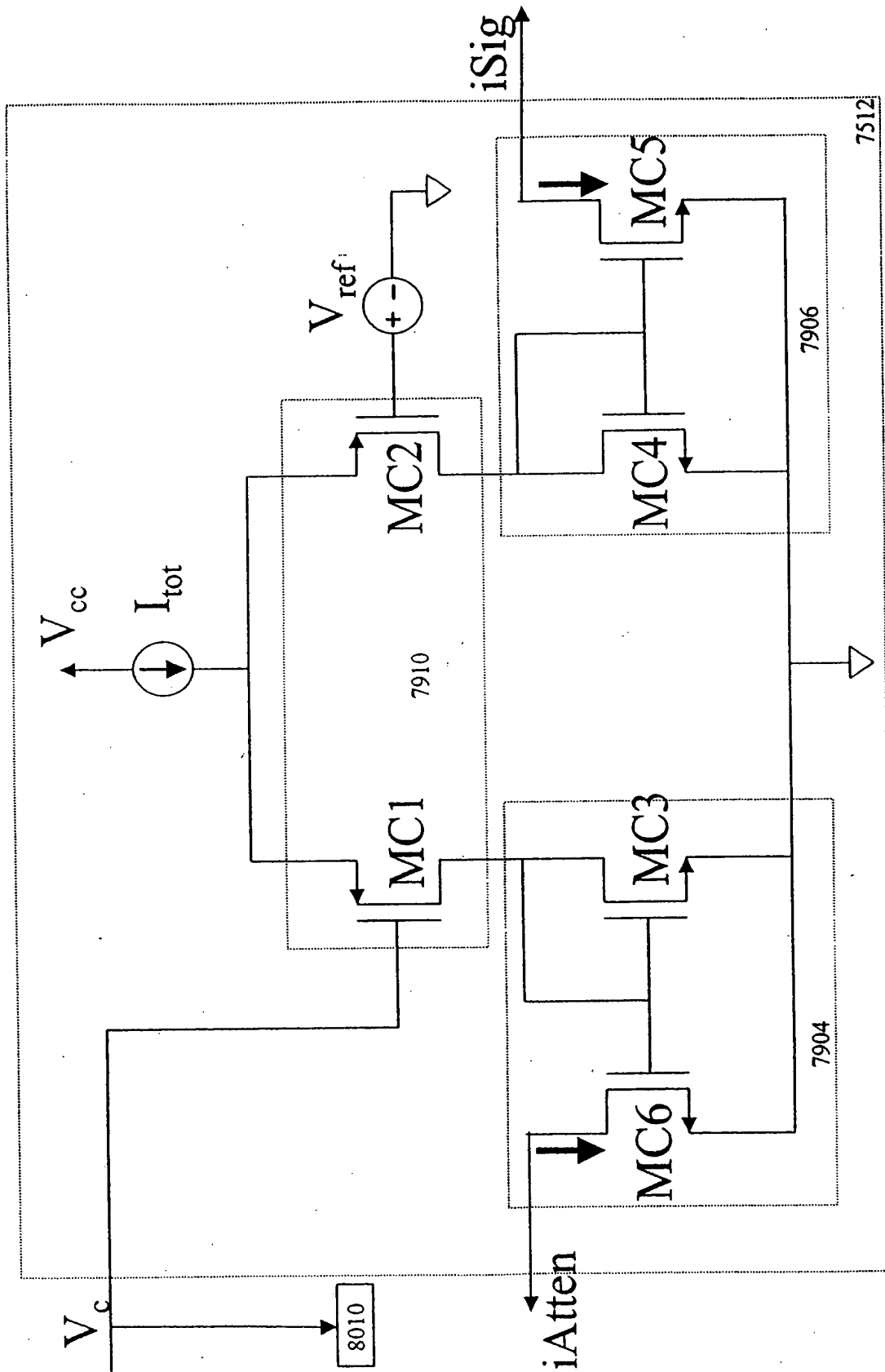


FIG. 79

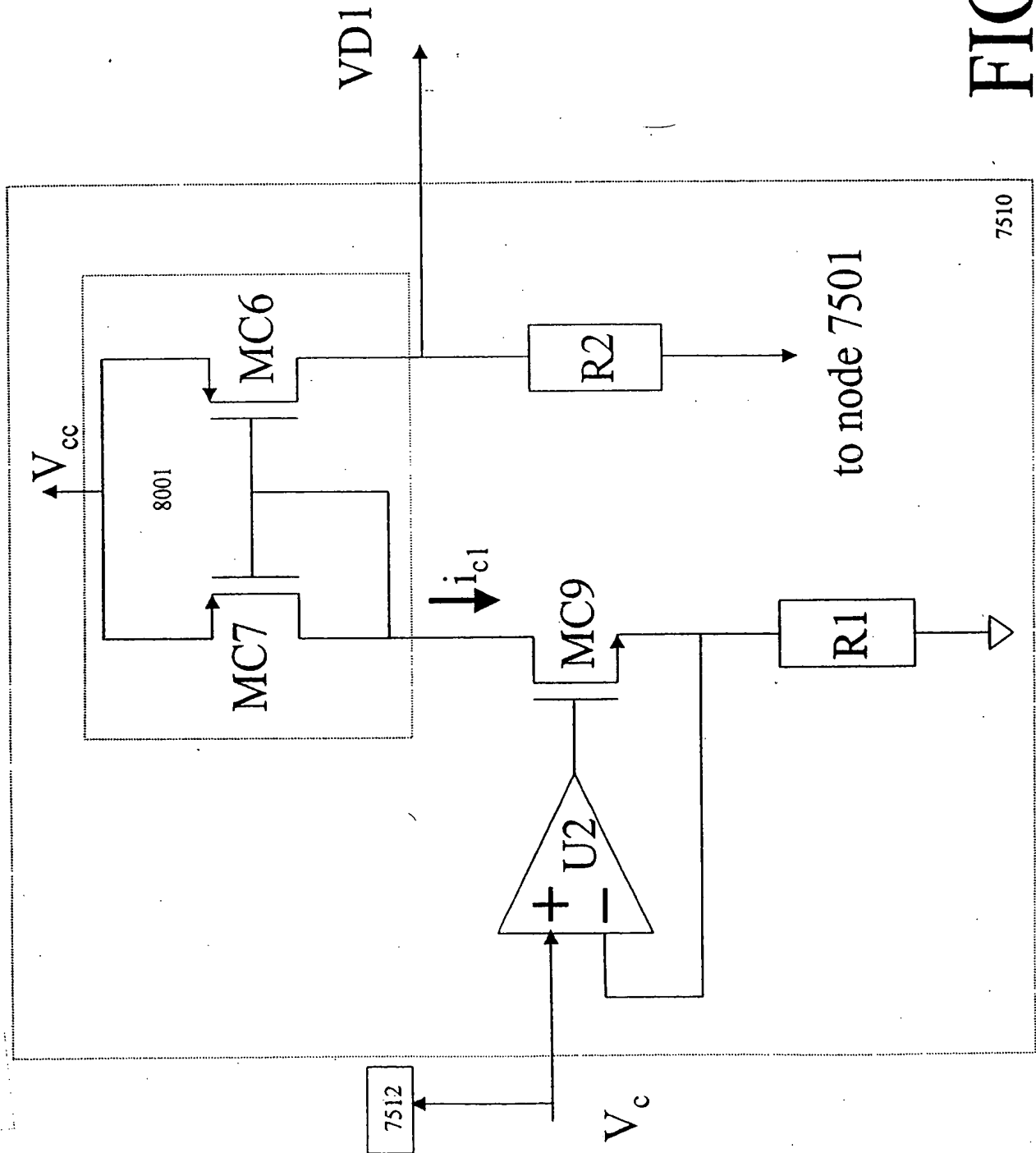


FIG. 80